Measuring Clock Jitter with xPC Target

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Introduction

Jitter can be defined as the deviation in a clock's output (e.g., timing edges, transitions, counts) from "ideal" positions or values. Any clocking source will have some amount of noise or jitter and these deviations can be leading or lagging the ideal. This article defines common jitter terms, measurements, and analysis techniques. To demonstrate applicability of these methods, xPC Target is used to characterize the clock jitter on a target PC. Namely, jitter measurements are modeled in Simulink and the model is run on a target PC booted with the xPC Target real-time kernel[1].

Three common jitter measurements are *period jitter*, *cycle-cycle jitter*, and *time interval error*. Period jitter is the deviation of each clock period from the ideal period. Cycle-cycle jitter is the change in adjacent clock periods and is computed by differencing the current and previous period. Time interval error (TIE) is the amount each clock cycle deviates from the ideal edge. TIE is difficult to measure since knowledge of the ideal edges is needed and usually unavailable. A sample "noisy" clock signal illustrating these concepts is plotted in Figure 1.

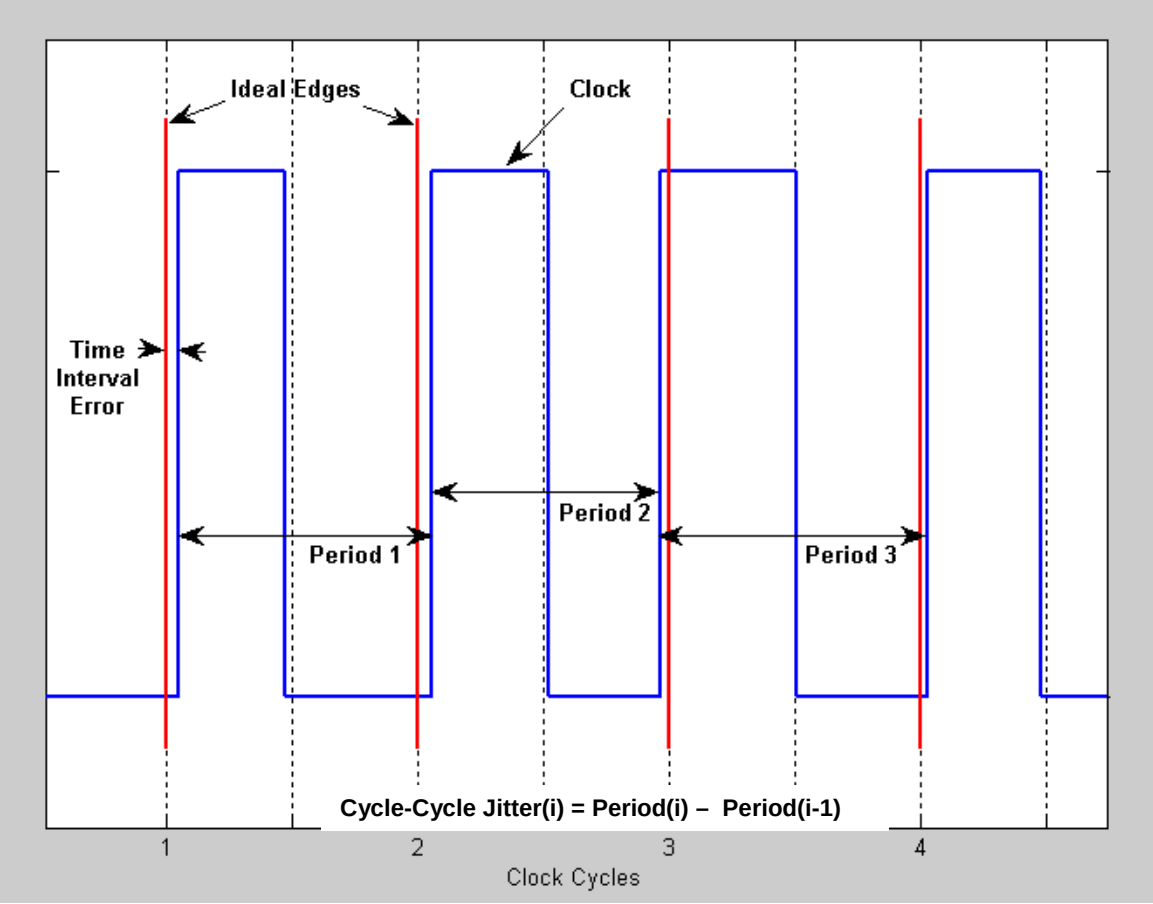

Figure 1. Clock with jitter.

[1] Accompanying Simulink models and MATLAB M-files were created and tested using xPC Target Version 3.3 (R2007b) with the Microsoft Visual Studio 2008 (vc8.0) compiler.

Measuring Clock Jitter with xPC Target

xPC Target provides two blocks that can be used to characterize and compute target PC clock jitter – the `Time Stamp Counter` and the `Time Stamp Delta` blocks which are found in the xPC Target Misc. library (See Figure 2). For Intel Pentium processors, the `Time Stamp Counter` block outputs a count of every CPU clock cycle via the Read Time-Stamp Counter (RDTSC) instruction. The output from two of these blocks can be input to the `Time Stamp Delta` block to compute the delta between the two time stamps.

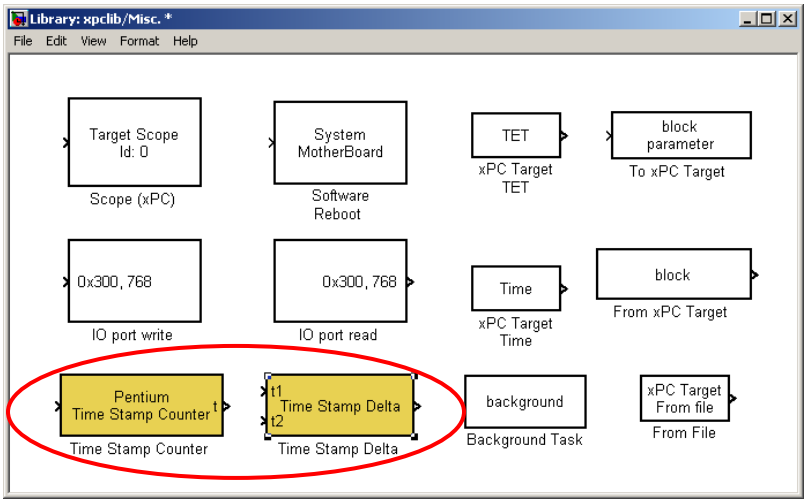

Figure 2. xPC Target™ Misc. library.

Using these blocks, a jitter measurement model can be constructed as shown in Figure 3. This model computes the period jitter[2] and cycle-cycle jitter in counts. It also computes a sample-by-sample estimate of the CPU clock frequency in Hertz. To convert the jitter signals from counts to time, divide by the clock frequency.

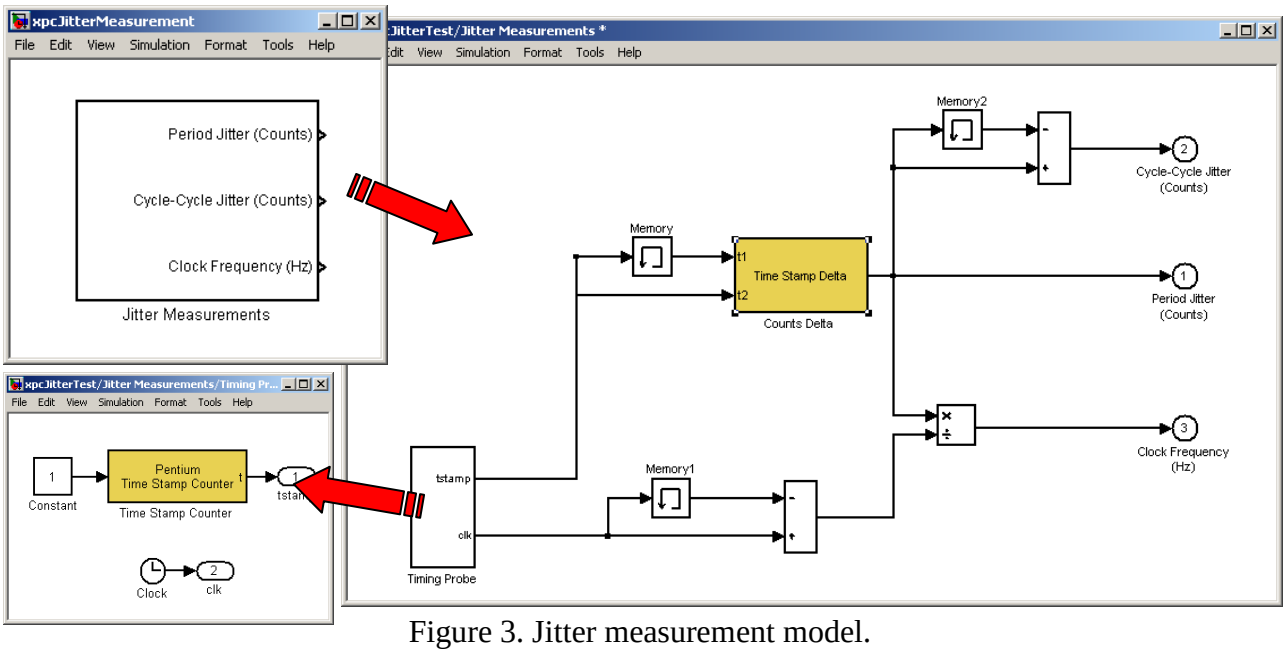

Figure 3. Jitter measurement model.

[2] Strictly speaking, period jitter is the "deviation" of each clock period from the ideal. In this model, and the analysis that follows, the term "period jitter" includes the ideal period (250 μs) as well.

Test Case

The jitter measurement model was inserted into the xPC Target shipping demo `xpcosc.mdl` and run on a target PC with a 2.8 GHz Pentium 4 processor. The model sample time is 250 µsec. A time history plot of the period jitter and cycle-cycle jitter along with the noise-free ideal values is shown in Figure 4.

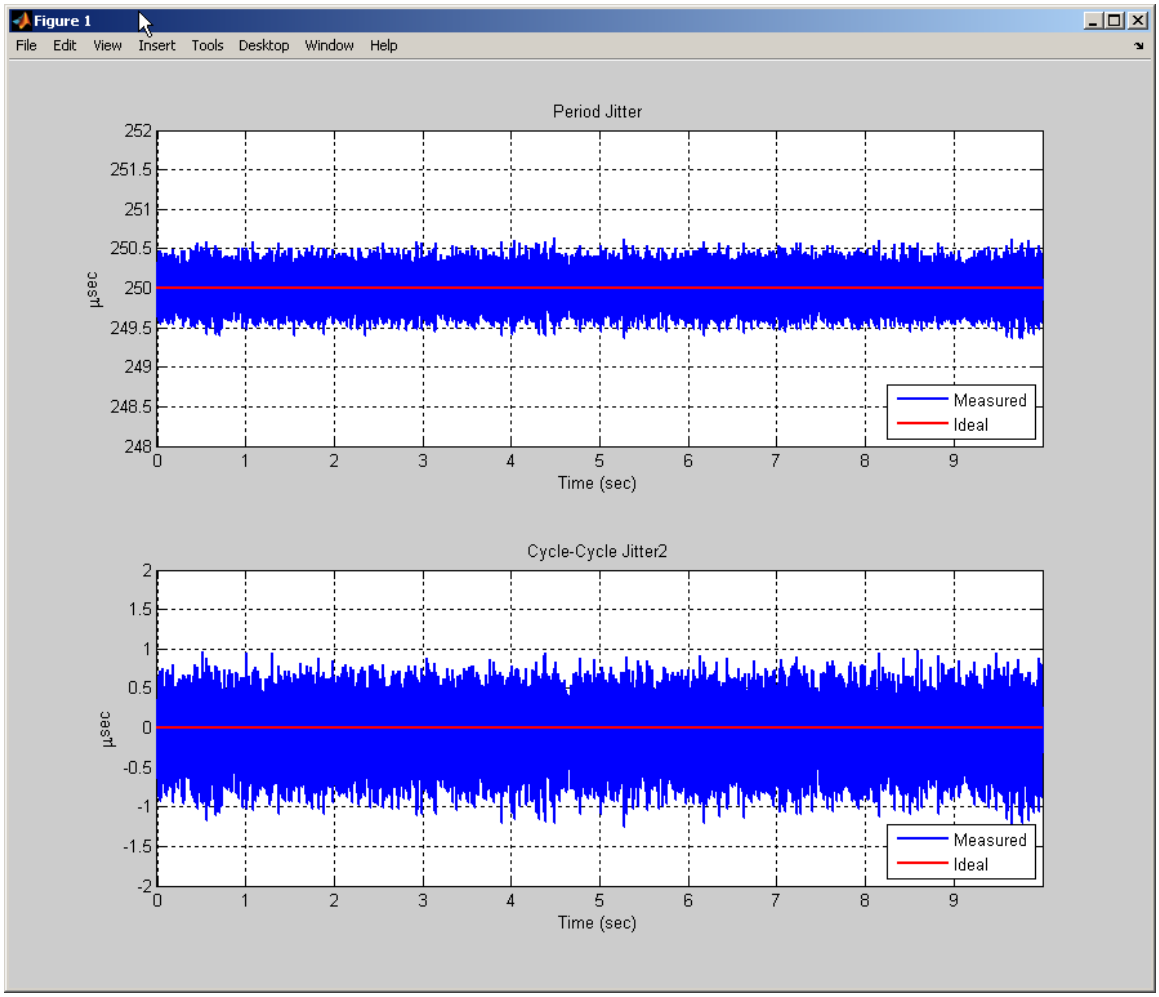

Figure 4. Jitter time history measurements.

Statistical Analysis

Statistical results from the test run are given below:

```
Clock Frequency Estimate (GHz): 2.790
Period Jitter Mean      (usec): 250.000
Period Jitter SDev      (usec): 0.165
Period Jitter Max       (usec): 250.633
Cycle-Cycle Jitter Mean (usec): 0.000
Cycle-Cycle Jitter SDev (usec): 0.292
Cycle-Cycle Jitter Max  (usec): 0.972
```

Notice the clock frequency estimate of 2.79 GHz is very close to the ideal. Also, both period and cycle-cycle jitter appear to be unbiased with fairly small (< 300 nsec) statistical deviations.

Histogram Analysis

Another interesting analysis tool is the histogram (see Figure 5). The histogram graphs a distribution of the jitter measurements and, for large data sets, is a good estimate of the probability density function (pdf) governing the noise process. Notice both histograms are Gaussian-like and that period jitter appears to have discrete periodic groupings.

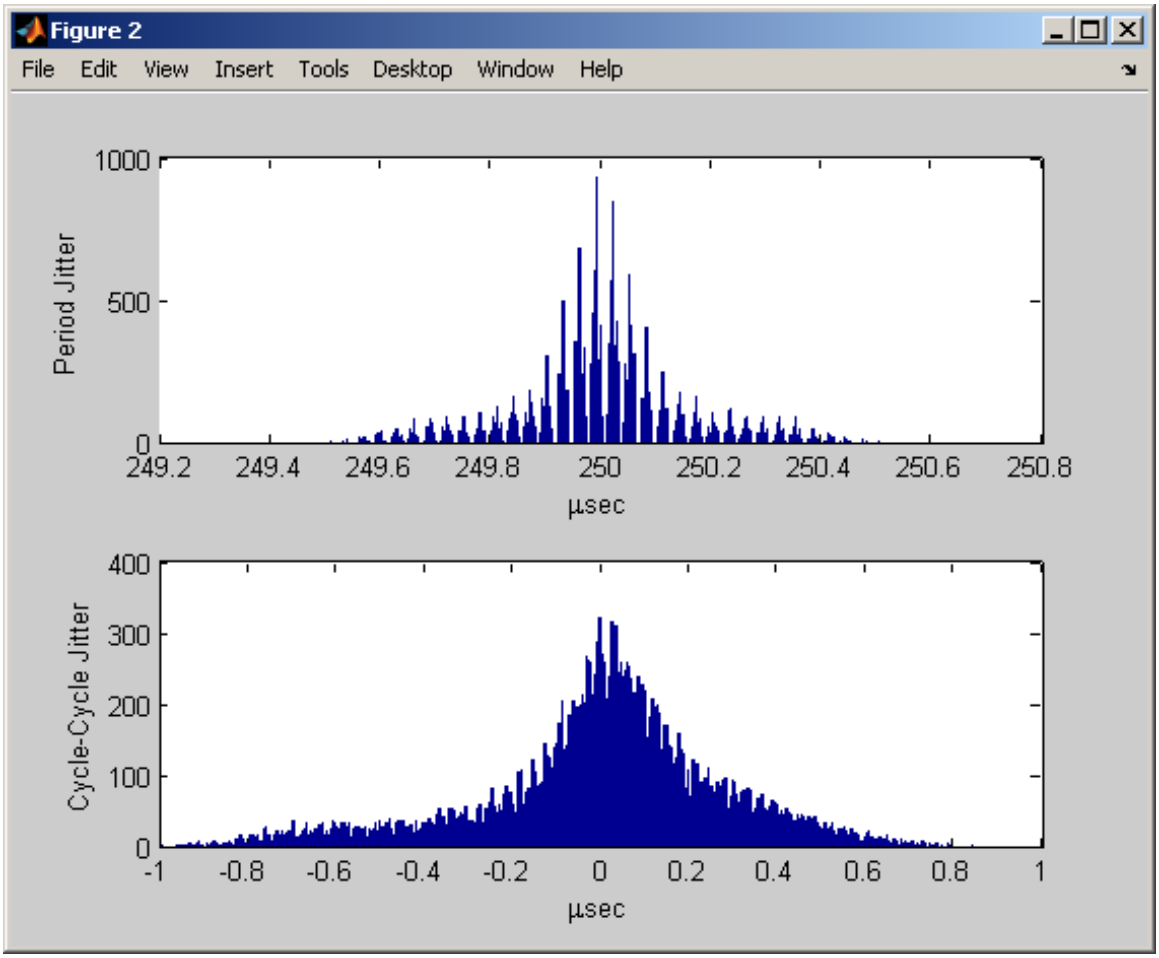

Figure 5. Jitter histograms.

Power Spectral Density Analysis

We can also look at the jitter measurements in the frequency domain. This has the advantage of revealing any periodic components in the data that might be masked in the time domain by the wideband noise. Figure 6 is a plot of the power spectrum for period jitter. As expected, this is a high frequency process. Timing variations that occur slowly (low frequency usually less than 10 Hz) are sometimes called *wander*.

The power spectrum also reveals harmonic components. These harmonics are closely associated with the cyclical clusters present in the histogram and are an indicator that a discrete element exists within the clock jitter.

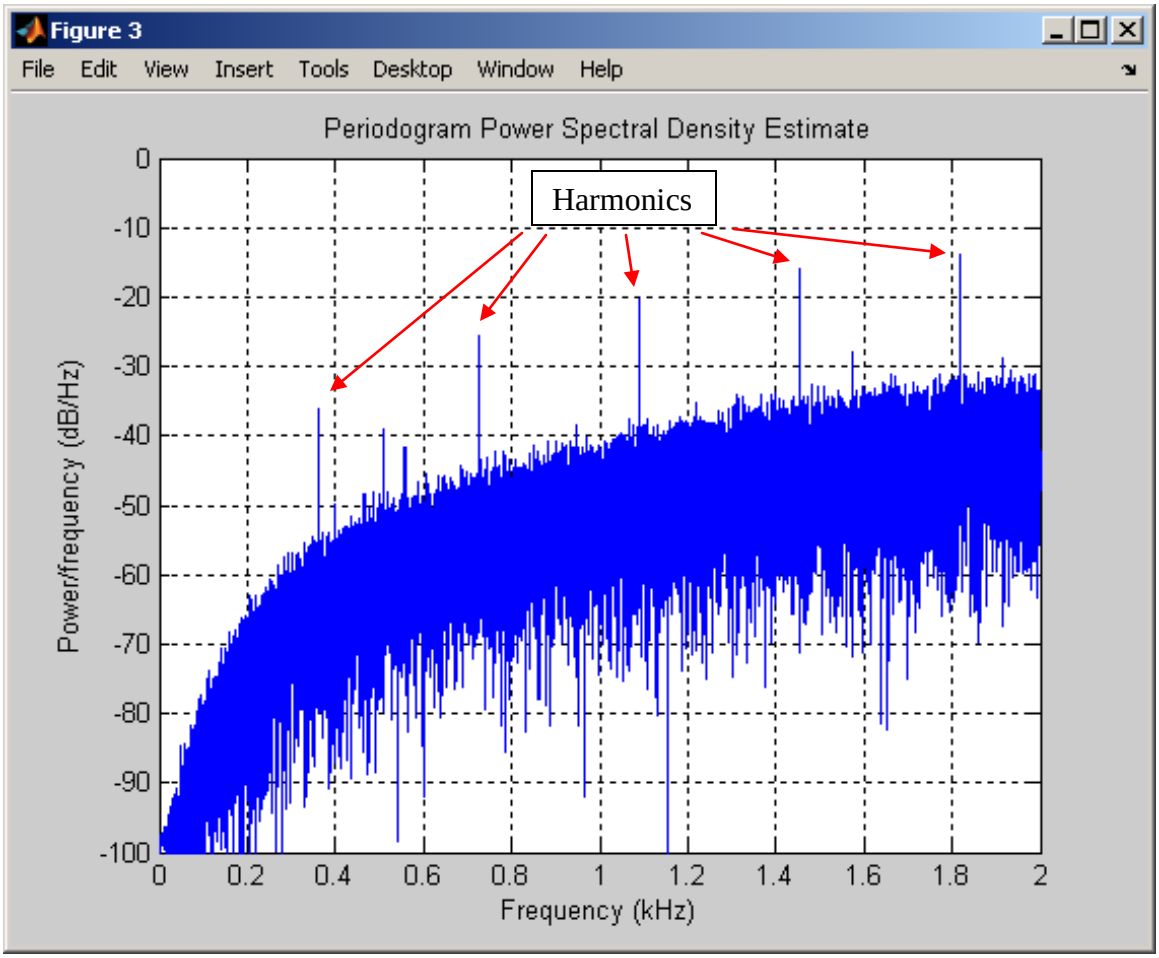

Figure 6. Period jitter power spectral density.

Conclusion

Jitter is random unwanted deviation in a clock's period or cycle. When timing is critical or when timing problems arise, it may be necessary to measure and characterize a clock's jitter. This article described several jitter measurement and analysis techniques. Finally, it was shown how these methods can be modeled in Simulink and tested with xPC Target to study PC clock jitter.