

# Filter Design HDL Coder 2.8

## Generate HDL code for fixed-point filters

Filter Design HDL Coder™ adds hardware implementation capability to MATLAB®. It lets you generate efficient, synthesizable, and portable VHDL® and Verilog® code for fixed-point filters that are designed with DSP System Toolbox, for implementation in ASICs or FPGAs. It also automatically creates VHDL and Verilog test benches for quickly simulating, testing, and verifying the generated code.

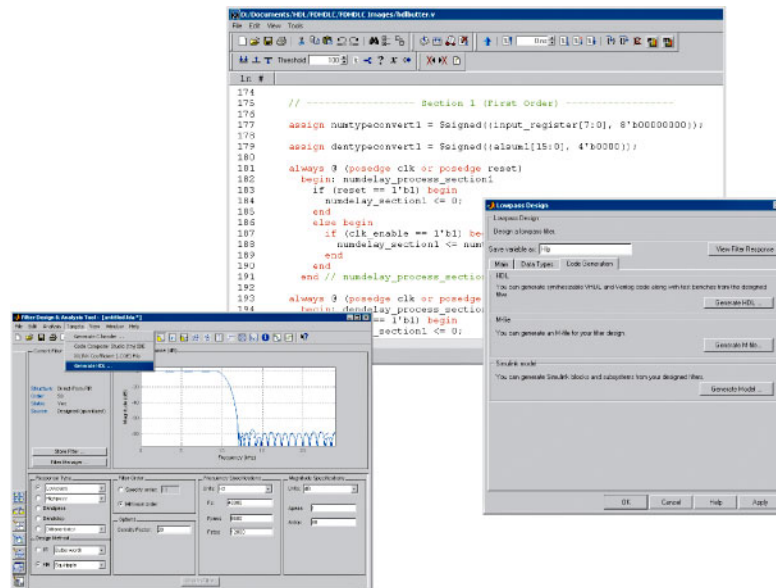
The generated VHDL and Verilog code adheres to a clean HDL coding style that enables architects and designers to quickly customize the code if needed. The test bench feature increases confidence in the correctness of the generated code and saves time spent on test bench implementation.

### Key Features

- Generates synthesizable IEEE 1076 compliant VHDL code and IEEE 1364-2001 compliant Verilog code for implementing fixed-point filters in ASICs and FPGAs
- Controls the content, optimization, and style of generated code
- Provides options for speed vs. area tradeoffs and architecture exploration, including distributed arithmetic
- Generates VHDL and Verilog test benches for quick verification and validation of generated HDL filter code
- Generates simulation and synthesis scripts

### Working with the Filter Design HDL Coder

Filter Design HDL Coder is integrated with the graphical user interface (GUI) and command line of DSP System Toolbox to provide a unified design and implementation environment. You can design filters and generate VHDL and Verilog code either from the MATLAB command line or from DSP System Toolbox using FilterBuilder or Filter Design and Analysis Tool (FDATool) GUIs.



Generating HDL code through the FDATool GUI.

## Designing Fixed-Point Filters

The design entry input to Filter Design HDL Coder is a quantized filter that you create in one of two ways:

- Design and quantize the filter with DSP System Toolbox
- Design the filter with Signal Processing Toolbox and then quantize it with DSP System Toolbox

Filter Design HDL Coder supports several important filter structures, including:

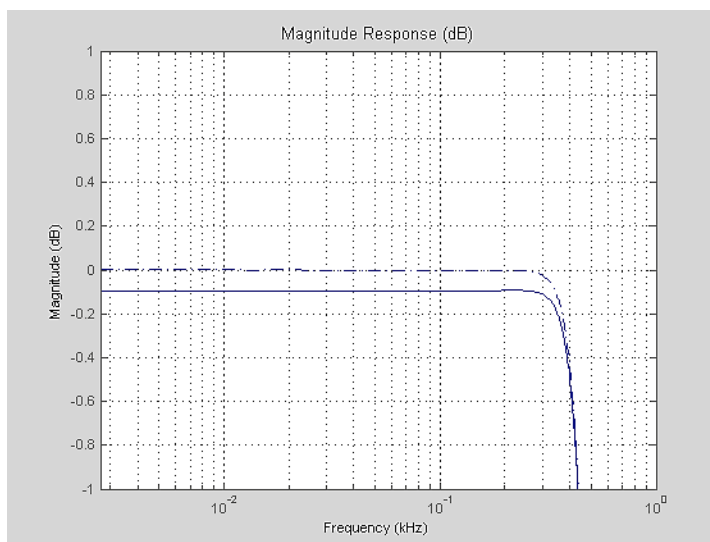
**Discrete-time finite impulse response (FIR)**, which includes symmetric, anti-symmetric, and transposed structures

**Second-order section (SOS) infinite impulse response (IIR)**, which includes direct form I, II, and transposed structures

**Multirate filters**, which includes cascaded integrator-comb (CIC) interpolator and decimator, direct-form FIR and transposed FIR polyphase interpolator and decimator, FIR hold and linear interpolator, and FIR polyphase sample rate converter structures

**Fractional delay filters**, which includes Farrow structures

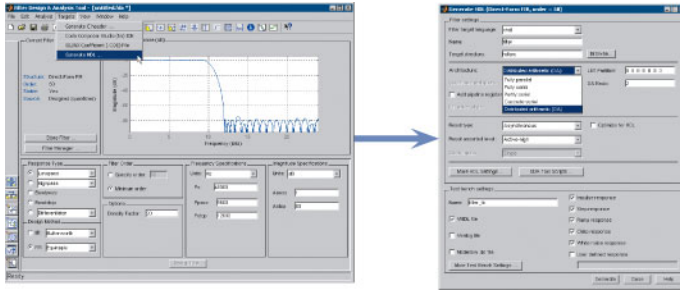
Filter Design HDL Coder can generate HDL code from cascaded multirate and discrete-time filters. Each of these single-rate and multirate filter structures supports fixed-point and floating-point (double precision) realizations. In addition, the FIR structures support unsigned fixed-point coefficients.



*Using DSP System Toolbox to prepare the filter design for code generation by quantizing, adjusting the scale values for, and re-quantizing the filter.*

## Generating HDL for Fixed-Point Filters

When you use the GUI to generate HDL code for fixed-point filters, all VHDL and Verilog output files are generated at the end of a dialog session. If the filter design requires a VHDL package, Filter Design HDL Coder also generates a package file. If you use the command line, the filter and test bench HDL files are generated separately.



Generate HDL GUI. After completing the design and quantization, you can specify options and generate the code and test benches with a single click.

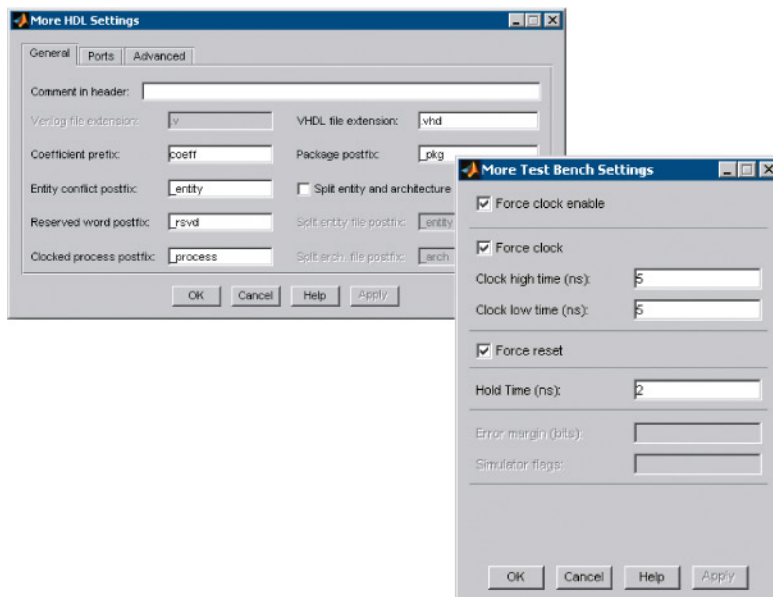
## Customizing VHDL and Verilog Code

Filter Design HDL Coder generates filter and test bench HDL code for a quantized filter based on an option setting or on property name and property value pairs. These settings let you:

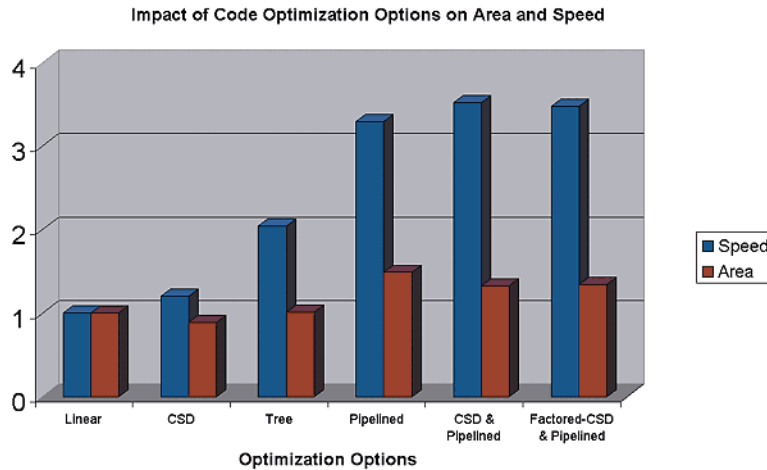
- Name language elements
- Specify port parameters
- Use advanced HDL coding features

All properties have default settings. You can customize the HDL output by adjusting the settings with the Filter Design HDL Coder dialog or the MATLAB command line. As an FDATool or FilterBuilder plug-in, the dialog enables you to set properties associated with:

- HDL language specification
- File name and location specifications
- Reset specifications
- HDL code optimizations
- Test bench customizations



Advanced options GUI for defining the characteristics of the generated code and specifying test benches.



*Performance and area metrics obtained for a 27 tap FIR filter for video applications. Optimization options provide insight into key implementation metrics.*

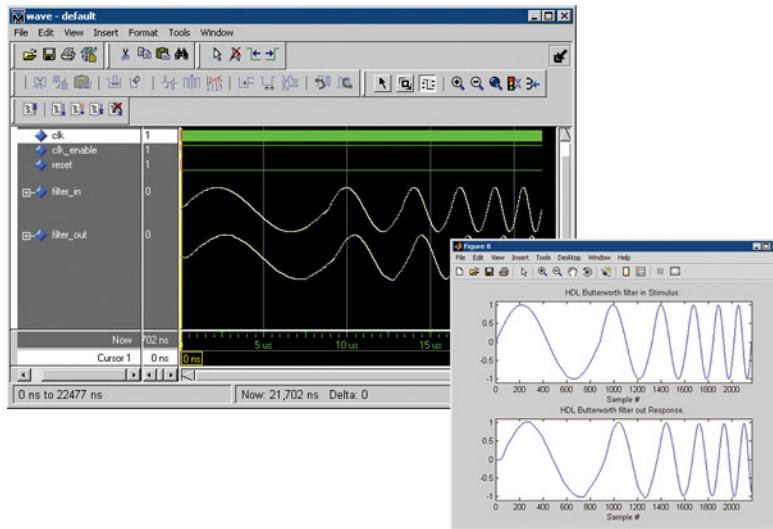
## Testing and Synthesizing Generated HDL Code

You can simulate and test the generated HDL code using the automatically generated VHDL and Verilog test benches. A MATLAB script can be generated for cosimulation using Link for ModelSim or Link for Cadence<sup>®</sup> Incisive<sup>®</sup> software (both available separately). This script automates the direct cosimulation of your filter design and the generated code, simplifying the task of comparing and verifying the results of the generated HDL code with the original filter design. This option enables you to utilize the advanced analysis and visualization capabilities of MATLAB to test, debug, and verify the HDL implementation of your filter designs.

## Architectural Optimizations

After quantizing the filter, you can use dialogs to invoke Filter Design HDL Coder and configure it with optimization, content, style, and test bench options for your filter application. Supported optimizations include:

- Canonical signed digit (CSD), for optimizing coefficient multiplier operations in the filter to reduce the area used and maintain or increase clock speed
- Speed vs. area tradeoff, for exploring hardware architectures for tradeoff between the chip area and the circuit operating frequency
- Distributed arithmetic (DA), for implementing FIR filters through a DA architecture without using multipliers
- In addition, Filter Design HDL Coder generates synthesis scripts that accelerate your synthesis work flow.



ModelSim simulation results of the fifth-order Butterworth filter and the original filter specification results from DSP System Toolbox. Automatically generated ModelSim test benches simplify and speed up the testing and verification of the VHDL and Verilog code generated by Filter Design HDL Coder.

## Resources

### Product Details, Demos, and System Requirements

[www.mathworks.com/products/filterhdl](http://www.mathworks.com/products/filterhdl)

### Trial Software

[www.mathworks.com/trialrequest](http://www.mathworks.com/trialrequest)

### Sales

[www.mathworks.com/contactsales](http://www.mathworks.com/contactsales)

### Technical Support

[www.mathworks.com/support](http://www.mathworks.com/support)

### Online User Community

[www.mathworks.com/matlabcentral](http://www.mathworks.com/matlabcentral)

### Training Services

[www.mathworks.com/training](http://www.mathworks.com/training)

### Third-Party Products and Services

[www.mathworks.com/connections](http://www.mathworks.com/connections)

### Worldwide Contacts

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