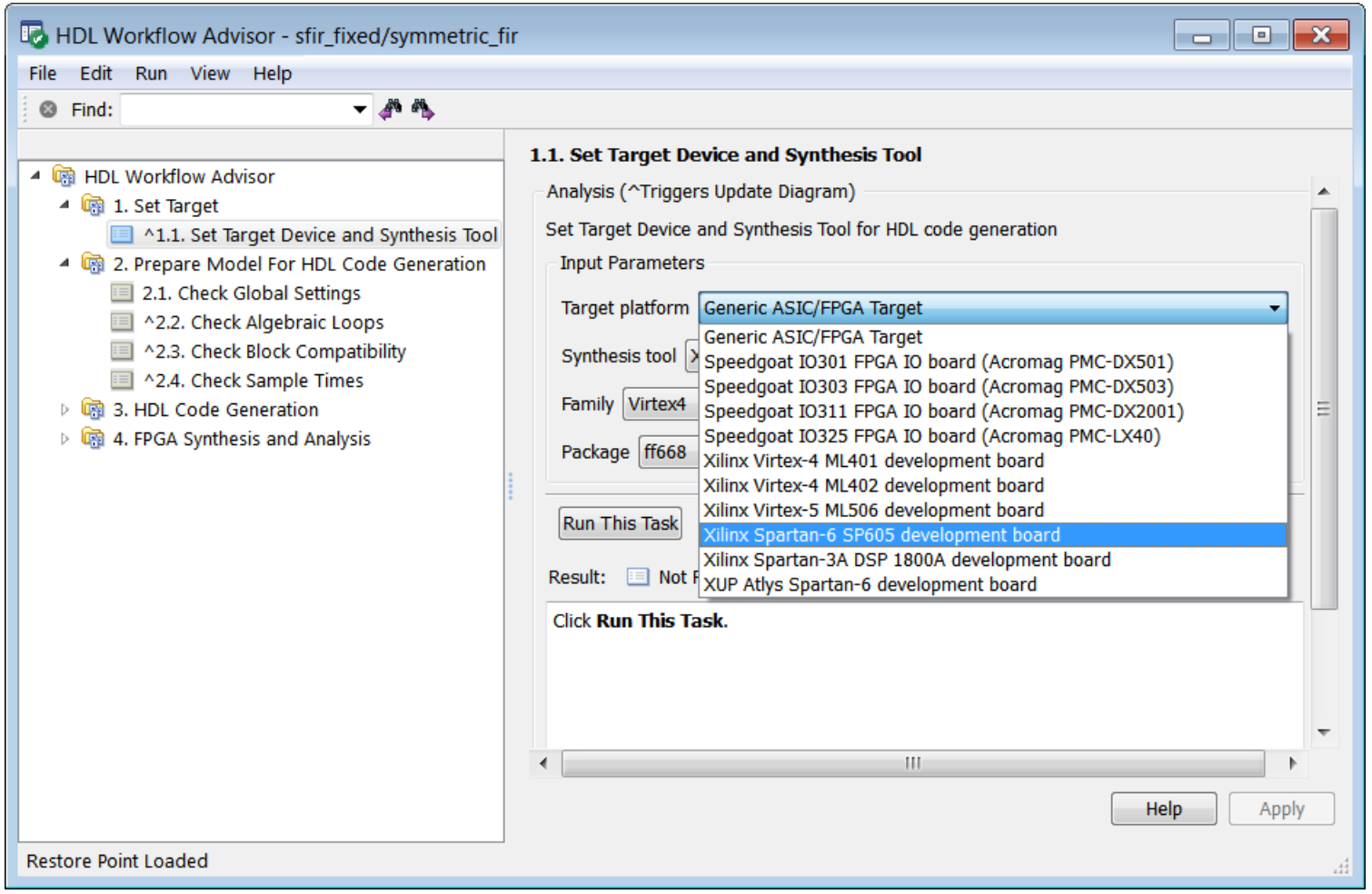
Latest Features in Simulink HDL Coder

R2011a

Rapid Prototyping for FPGA Boards

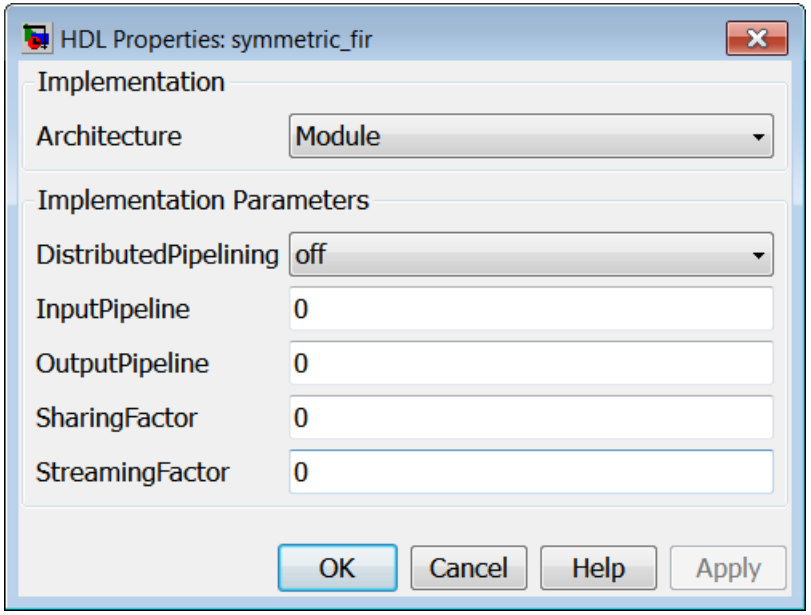
Generate HDL code for ASIC, FPGA, or vendor boards



Enhanced Optimizations

Pipelining, resource sharing, and multichannelization

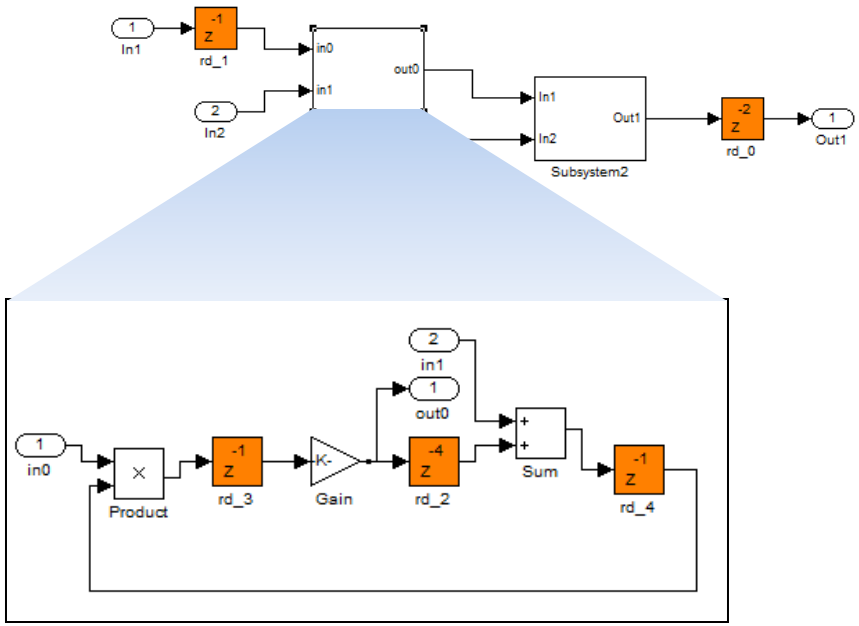
- Perform area-speed optimization with:
  - Pipelining
  - Resource sharing
  - Multichannelization



Enhanced Optimizations

Distributed pipelining inside subsystems

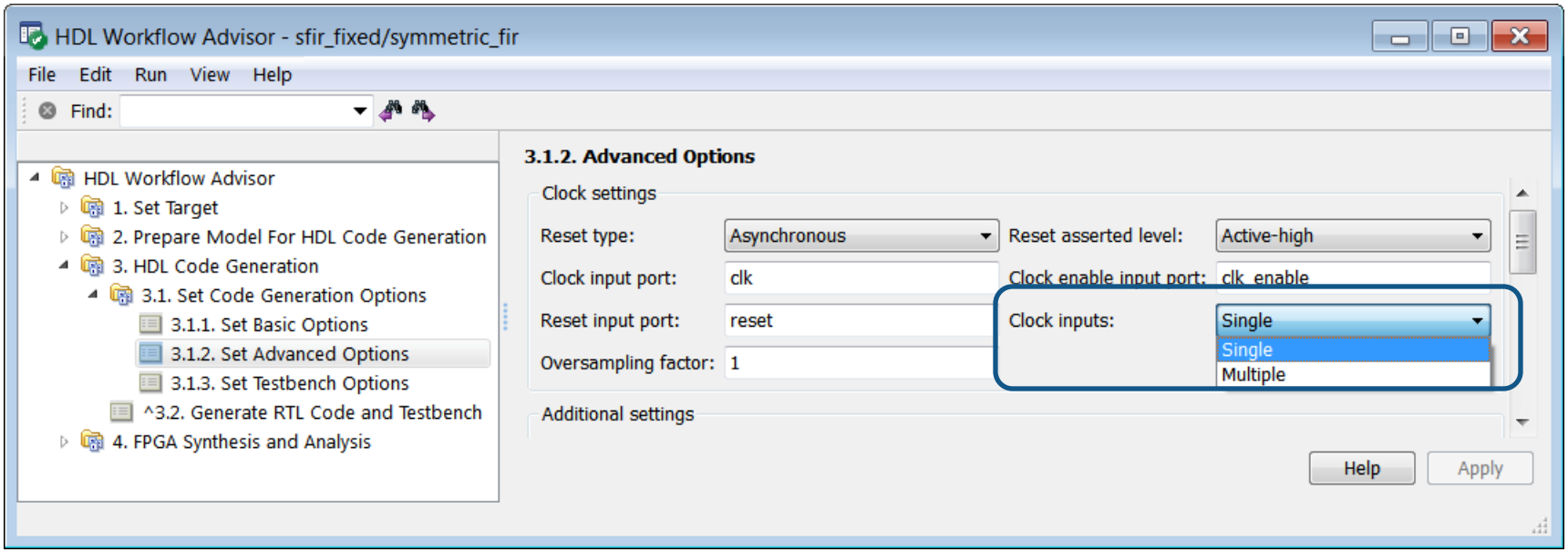
- Use distributed pipelining with:
  - Hierarchical designs
  - Feedback loops



Multiclock Support in Simulink HDL Coder

Create designs with multiple synchronous clocks

- New clocking options:
  - Single clock
  - Multiple synchronous clocks



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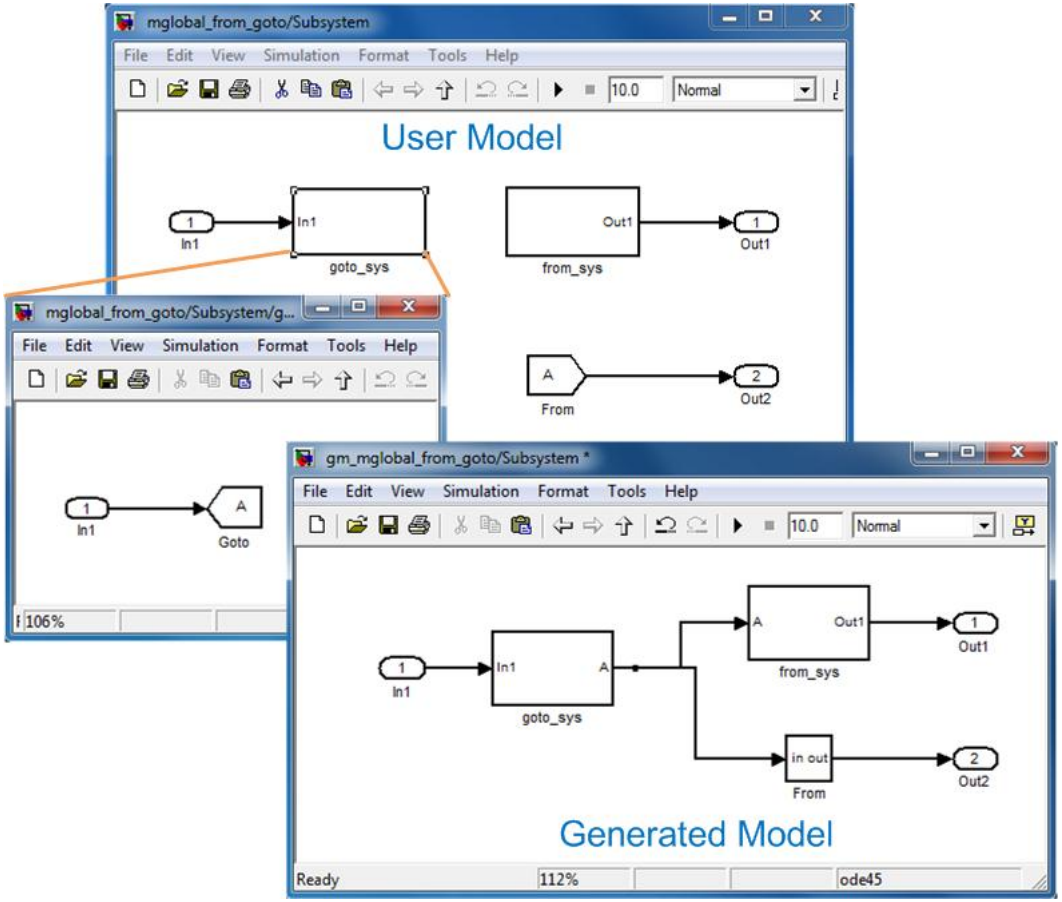
Support for Goto/From Blocks

New block support



Support for RAM-Based Viterbi Decoder

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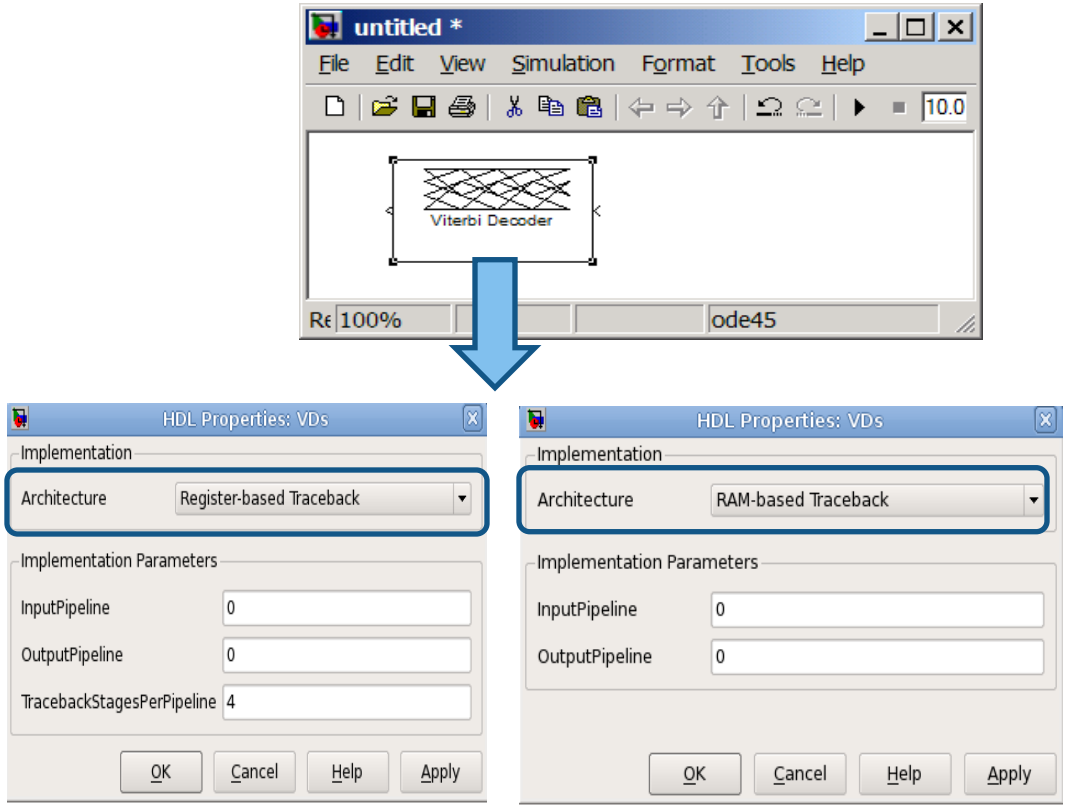
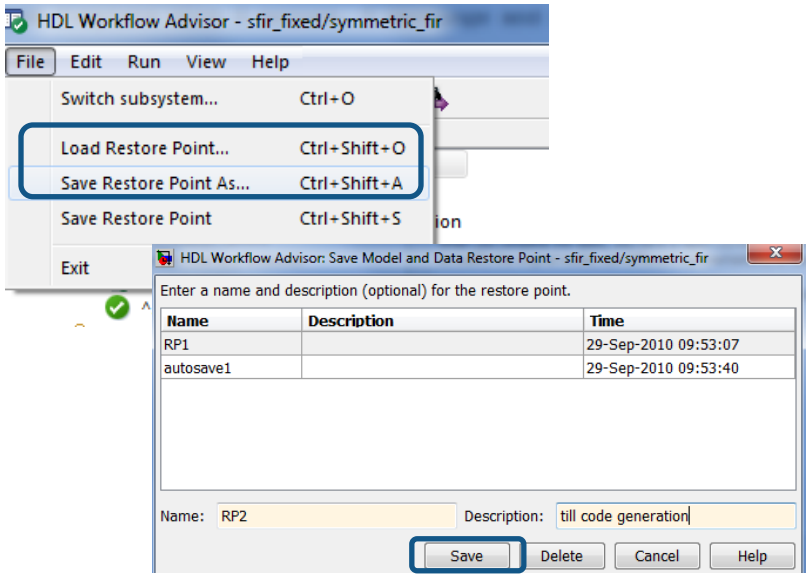
Generate register or RAM-based HDL traceback unit for Viterbi decoder block



Save and Restore Feature in Workflow Advisor

Save current HDL Workflow Advisor session and recover previously stored sessions



Support for Generics in Black-Box Interface

Use black-box interface to import existing HDL IP containing *generics*