

Latest Features in Simulink HDL Coder

R2011a

Rapid Prototyping for FPGA Boards

Generate HDL code for ASIC, FPGA, or vendor boards

The screenshot displays the HDL Workflow Advisor window for a project named 'sfir_fixed/symmetric_fir'. The interface includes a menu bar (File, Edit, Run, View, Help) and a search field. The left pane shows a tree view of the workflow steps:

- HDL Workflow Advisor
 - 1. Set Target
 - 1.1. Set Target Device and Synthesis Tool (selected)
 - 2. Prepare Model For HDL Code Generation
 - 2.1. Check Global Settings
 - 2.2. Check Algebraic Loops
 - 2.3. Check Block Compatibility
 - 2.4. Check Sample Times
 - 3. HDL Code Generation
 - 4. FPGA Synthesis and Analysis

The main workspace shows the details for task '1.1. Set Target Device and Synthesis Tool'. It includes an analysis section and input parameters:

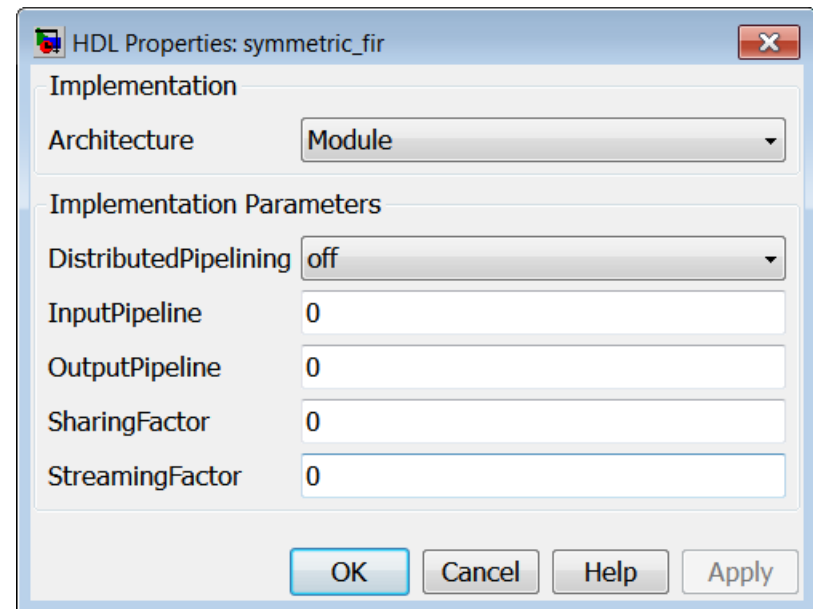
- Analysis (^Triggers Update Diagram)
 - Set Target Device and Synthesis Tool for HDL code generation
- Input Parameters
 - Target platform: Generic ASIC/FPGA Target (dropdown menu is open, showing a list of boards including Xilinx Spartan-6 SP605 development board)
 - Synthesis tool: Generic ASIC/FPGA Target
 - Family: Virtex4
 - Package: ff668

Buttons for 'Run This Task', 'Help', and 'Apply' are visible at the bottom. A status bar at the bottom left indicates 'Restore Point Loaded'.

Enhanced Optimizations

Pipelining, resource sharing, and multichannelization

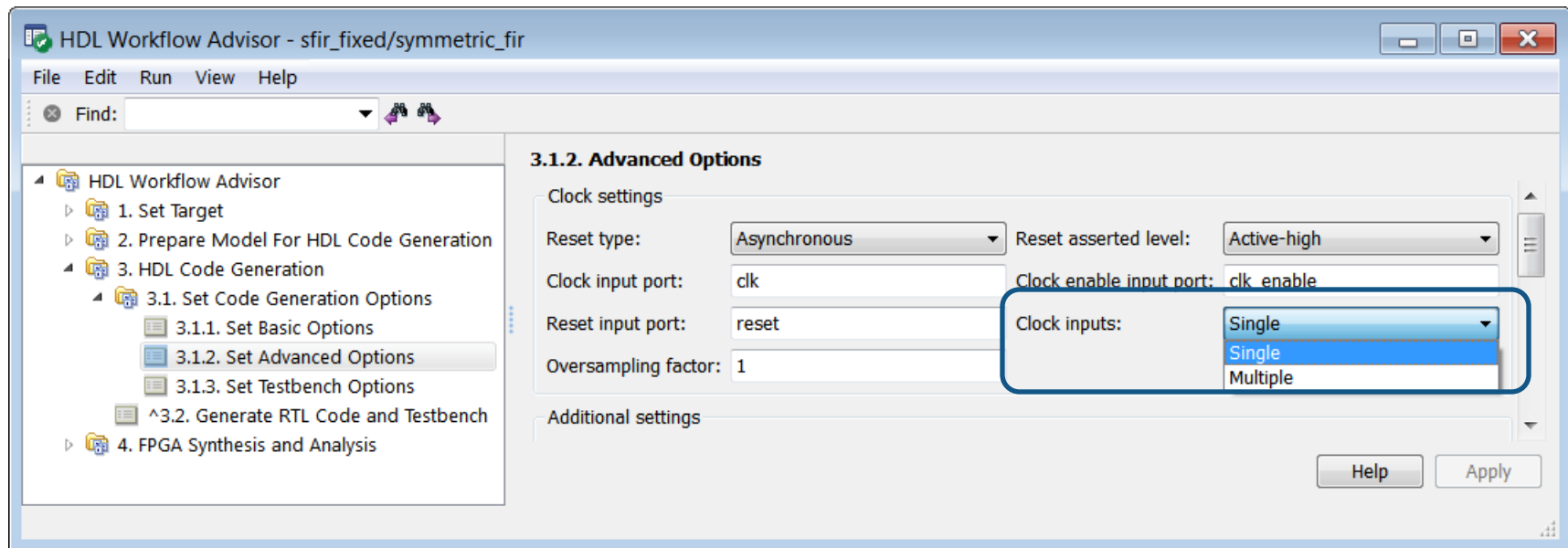
- Perform area-speed optimization with:
 - Pipelining
 - Resource sharing
 - Multichannelization



Multiclock Support in Simulink HDL Coder

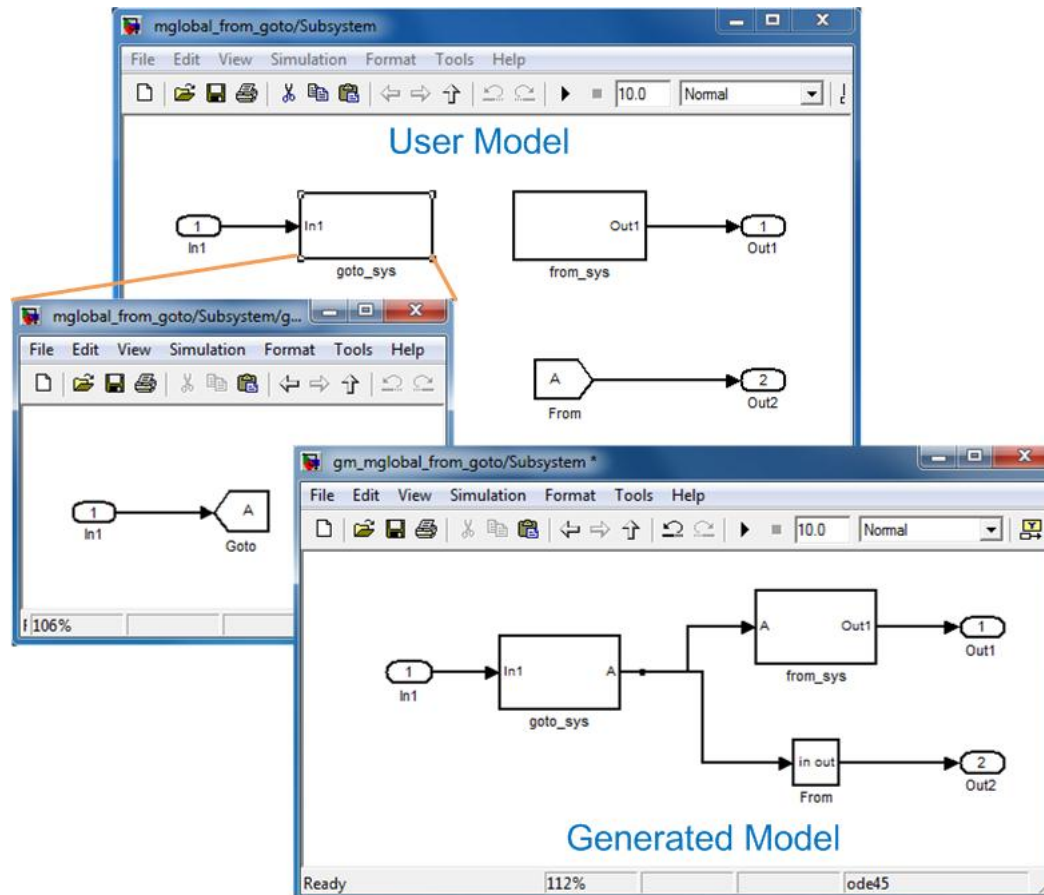
Create designs with multiple synchronous clocks

- New clocking options:
 - Single clock
 - Multiple synchronous clocks



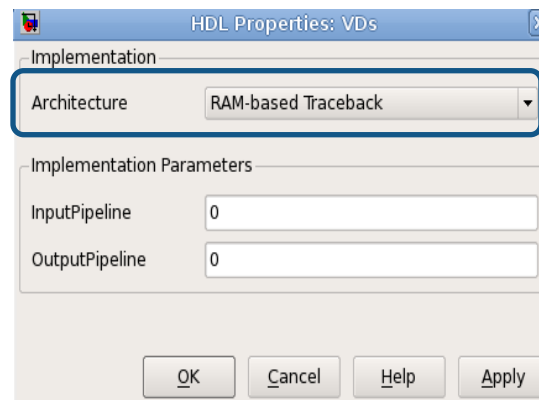
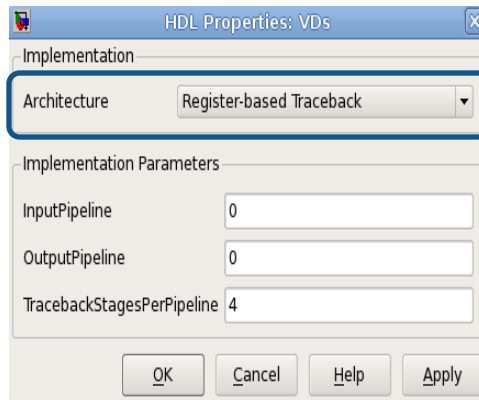
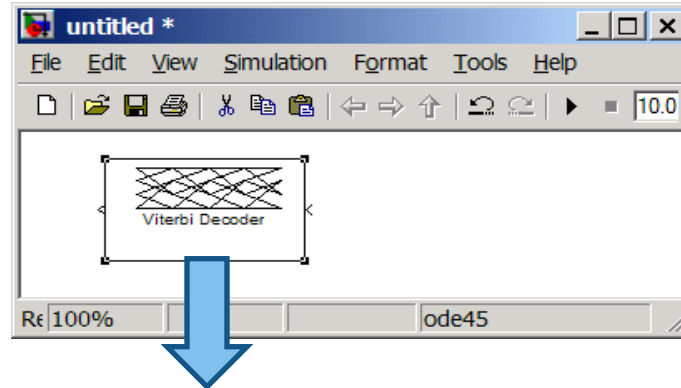
Support for Goto/From Blocks

New block support



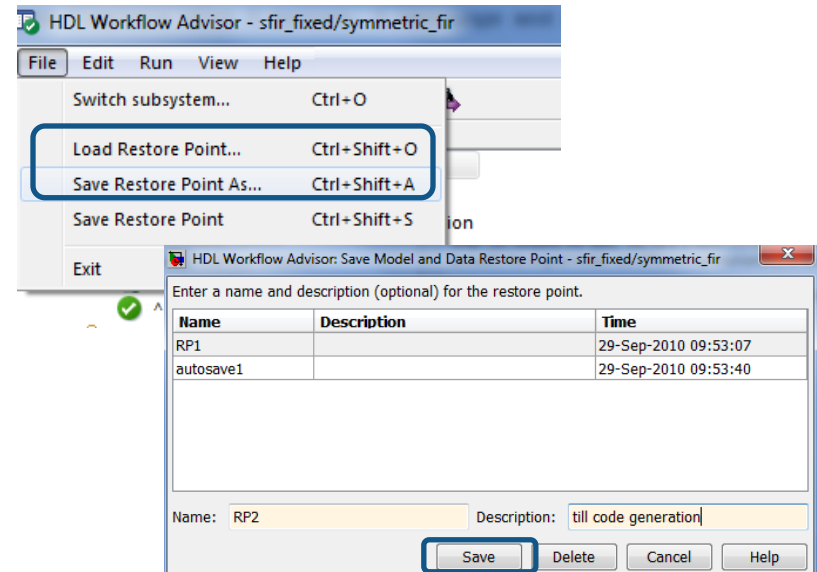
Support for RAM-Based Viterbi Decoder

Generate register or RAM-based HDL traceback unit for Viterbi decoder block



Save and Restore Feature in Workflow Advisor

Save current HDL Workflow Advisor session and recover previously stored sessions



Support for Generics in Black-Box Interface

Use black-box interface to import existing HDL IP containing *generics*

