MathWorks®
Accelerating the pace of engineering and science

HDL Code Generation Onboarding Program

The HDL Code Generation Onboarding program is a learning path designed to help engineers ramp up on generating HDL Code from ***Simulink***® blocks, ***MATLAB***® code, and ***Stateflow***® charts.. The program features a variety of resources including videos, self-paced training, webinars and on-site sessions.

To request on-site training or for more information, contact your account manager.

Category	Activity	Duration	Resource Type	Cost
Phase 1: Fundamentals of Model-Based Design	Introduction to MATLAB Onramp	45 min.	***Online Video***	Complimentary
	Simulink Overview	2 min. each	***Online Video*** #1 ***Online Video*** #2	Complimentary
	Introduction to Simulink Onramp	1 hr	***Video series***	Complimentary
	Modeling and Simulation Made Easy with Simulink	30 min.	***Online Video***	Complimentary
	MATLAB Fundamentals	1 day	Onsite training Or Self-paced Online	***Fee-based training***
	Simulink Fundamentals	2 days	Onsite training- Days 2-3 of 5 day	***Fee-based training***
	Stateflow Fundamentals	2 days	Onsite training- Days 4-5 of 5 day	***Fee-based training***
	Getting Started with Simulink / Stateflow	(2) 1 hr. sessions	MathWorks Engineer Onsite	Complimentary

	Getting Started with Simulink	N/A	***documentation***	Complimentary
Phase 2: Modeling Environment and Deployment to FPGA's	Design and Verification of FPGA and ASIC Applications	40 min.	***On Line Video***	Complimentary
	Designing for HDL Code Generation	8 min.	***Online Video***	Complimentary
	HDL Implementation and Verification of a High-Performance FFT	25 min.	***On-Line Video***	Complimentary
	HDL Coder Self-Guided Tutorial	N/A	***Free Download***	Complimentary
	Methodology guide for learning and evaluating HDL Coder	N/A	Documentation and examples (***download***)	Complimentary
	Training Class: FPGA and hardware design for DSP Engineers	3 days	(***Link***) for Details	Fee Based
	Technical Seminar: Introduction to HDL Coder and HDL Verifier	2 hrs.	MathWorks Engineer Onsite	Complimentary
	Technical Seminar: Signal	2 hours	MathWorks Engineer Onsite	Complimentary

	Processing Design for FPGAs: A Model-Based Approach			
	Generating HDL Code from Simulink	2 days	On-site training	***Fee-based training***
	HDL Coder Documentation	N/A	***Documentation: HDL Verifier***	Complimentary
Phase 3: Verification of VHDL and Verilog	What is HDL Verifier	2 min.	***Online Video***	Complimentary
	Improve RTL Verification by Connecting to MATLAB	40 min.	***Online Video***	Complimentary
	Generating a UVM verification checker model	5 min.	***Online Video***	Complimentary
	Import HDL for Cosimulation with Simulink	5 min.	***Online video***	Complementary
	Using Custom Boards for FPGA-in-the-Loop Verification	2 min.	***Online Video***	Complimentary
	HDL Verifier: FPGA Data Capture	4 min.	***Online Video***	Complimentary
	MATLAB as AXI Master with Xilinx FPGA and	5 min.	***Online Video***	Complimentary

	Zynq SoC Boards			
	HDL Verifier Documentation	N/A	***Documentation: HDL Verifier***	Complimentary
Phase 4: System on a Chip (SoC), and Application-Specific Topics	Programming Intel SoC FPGAs with Embedded Coder and HDL Coder	13 min.	***Online Video***	Complimentary
	Getting Started with Software-Defined Radio using MATLAB and Simulink	22 min.	***Online Video***	Complimentary
	Verify Xilinx RFSoC System Performance with MATLAB and Simulink	18 min.	***Online Video***	Complimentary
	Vision Processing for FPGA	5 x 5 min. videos	***Online Video Series***	Complimentary
	CPU, FPGA, and I/O Solutions for Real-Time Simulation and Testing with Simulink	16 min.	***Online Video***	Complimentary
	Hardware-in-the-Loop (HIL) Simulation for Power Electronics	26 min.	***Online Video***	Complimentary

	Systems			
	Programming Xilinx Zynq SoCs with MATLAB and Simulink	2 days	Onsite training 2 days	Fee based
	Software-Defined Radio Prototyping with Simulink	2 hours	MathWorks Engineer Onsite	Complimentary