Hardware-Software Co-Design and Prototyping on SoC FPGAs

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Agenda

- **Integrated Hardware / Software Top down Workflow for SoC FPGA’s, highlighting:**
  - Model Based Design Workflow for SoC FPGA’s
  - Automatic Code Generation:
    - HDL code generation for the FPGA fabric and C-Code generation for the ARM MCU
  - Automatic Interface Logic Generation:
    - Generation of the interface logic and software between the FPGA and ARM.
  - Integrated Verification:
    - Integrated HDL Verification using HDL Co-simulation and FPGA-in-Loop

- Next Steps, Q&A
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- Next Steps, Q&A
Edge Detection Demo – Behavioral Model
Edge Detection Demo – Implementation Model
You May Have Some Questions?

- How can we:
  - Implement designs on SoC FPGA’s?
  - Partition the HW and SW?
  - Generate the Interface Logic?
Design Challenges for Soc FPGA’s

- **FPGA Designers** not familiar with programming processors
- **DSP/Processor programmers** not familiar with FPGAs
- What should run on the FPGA vs. what should run on the ARM?
- No established rules for hooking up the interface between FPGA and ARM processor
Model-Based Design
Why Model-Based Design?

Requirements Development
Simulation
Code Generation
Continuous Verification
Model-Based Design:

From Concept to Production

- Automate regression testing
- Detect design errors
- Support certification and standards
- Generate efficient code
- Explore and optimize implementation tradeoffs
- Model multi-domain systems
- Explore and optimize system behavior in floating point and fixed point
- Collaborate across teams and continents
- Automate regression testing
- Detect design errors
- Support certification and standards
SoC FPGA Design Flow

User defines partitioning

MathWorks automates code and interface-model generation

MathWorks automates the build and download through the FPGA tools
Model-Based Design for SoC FPGA
Solution: C and HDL Code Generation

- Design, execute, and verify algorithms in MATLAB
- Automatically generate C or HDL code
- Deploy generated code on hardware
Code Generation Products for VHDL/Verilog

HDL Coder™
Automatically generate VHDL or Verilog from MATLAB code and Simulink Model

MATLAB® Coder™
Automatically generate C and C++ from MATLAB code

Fixed-Point Designer™
provides fixed-point data types and arithmetic
Code Generation Products for C/C++

- **MATLAB® Coder™**
  Automatically generate C and C++ from MATLAB code

- **Simulink® Coder™**
  Automatically generate C and C++ from Simulink models and Stateflow charts

- **Embedded Coder™**
  Automatically generate C and C++ optimized for embedded systems
Edge Detection Demo – Behavioral Model
Workflow for Video Image Processing

Concept Development

Algorithm Development

Prototyping

Architecture design

Prototyping

Chip design

Frame based

Image/Video Engineer

Pixel based

HW Engineer
Vision HDL Toolbox

*Design and prototype video image processing systems*

- **Modeling hardware behavior of the algorithms**
  - Pixel-based functions and blocks
  - Conversion between frames and pixels
  - Standard and custom frame sizes

- **Prototyping algorithms on hardware**
  - Efficient and readable HDL code
  - FPGA-in-the-loop testing and acceleration
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- Next Steps, Q&A
HW-SW Co-Design: It’s all about the Workflow

Prepare model for IP core generation
Configure Interface Logic
RTL Code Generation for IP Core
Generate Software/Hardware Model
Synthesis/ Bit File Generation
Deployment
Model-Based Design flow using MATLAB/Simulink
from Algorithm to FPGA Implementation

MATLAB® and Simulink®
Algorithm and System Design

HDL Coder
RTL Creation

HDL Verifier
HDL Co-Simulation

RTL
Back Annotation

Implement Design
Synthesis
Map
Place & Route

Verification
Functional Simulation
Static Timing Analysis
Timing Simulation

HDL Verifier
FPGA in the Loop

Design
Algorithm Development
MATLAB Simulink Stateflow
SoC FPGA Model-Based Design Workflow
SoC FPGA Model-Based Design Workflow

MATLAB® and Simulink®
Algorithm and System Design

Simulink Model
Configure Interface Logic

- Prepare model for IP core generation
- Configure Interface Logic
- RTL Code Generation for IP Core
- Generate Software/Hardware Model
- Synthesis/Bit File Generation
- Deployment
RTL Code Generation for IP Core

1. Prepare model for IP core generation
2. Configure Interface Logic
3. RTL Code Generation for IP Core
4. Generate Software/Hardware Model
5. Synthesis/Bit File Generation
6. Deployment
Full Bidirectional traceability
SoC FPGA Model-Based Design Workflow

MATLAB® and Simulink®
Algorithm and System Design

HDL IP Core
Generation

Programmable Logic IP Core
Algorithm from
MATLAB/ Simulink

AXI4-Stream Video In
AXI4-Stream Video Out
External Ports

AXI Lite Accessible Registers

HDL IP Core
Generation

HW
SW
SoC FPGA Model-Based Design Workflow

MATLAB® and Simulink® Algorithm and System Design

HDL IP Core Generation

EDK Integration

FPGA Bitstream

Zynq Platform

EDK Project

AXI Lite Accessible Registers

Algorithm from MATLAB/ Simulink

Programmable Logic IP Core

AXI4-Stream Video In

AXI4-Stream Video Out

External Ports

Processing System

AXI Video DMA

AXI Lite Accessible Registers

Algorithm from MATLAB/ Simulink

Programmable Logic IP Core

External Ports

EDK Integration
Generate Software/Hardware model

- Prepare model for IP core generation
- Configure Interface Logic
- RTL Code Generation for IP Core
- Generate Software/Hardware Model
- Synthesis/ Bit File Generation
- Deployment
SoC FPGA Model-Based Design Workflow

MATLAB® and Simulink® Algorithm and System Design

HDL IP Core Generation

EDK Integration

SW Interface Model Generation

FPGA Bitstream

SW Build

Zynq Platform

## MATLAB® and Simulink® Algorithm and System Design

HDL IP Core Generation

EDK Integration

SW Interface Model Generation

FPGA Bitstream

SW Build

Zynq Platform

## HDL IP Core Generation

MATLAB® and Simulink® Algorithm and System Design

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EDK Integration

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## SW Interface Model

MATLAB® and Simulink® Algorithm and System Design

HDL IP Core Generation

EDK Integration

SW Interface Model Generation

FPGA Bitstream

SW Build

Zynq Platform

## SW Interface Model
SoC FPGA Model-Based Design Workflow

- Real-time Parameter Tuning and Verification
  - External Mode
  - Processor-in-the-loop
Fast Prototyping and Iteration

Fast prototyping, iteration, and live probing/tuning directly on SoC FPGA hardware
Zynq HW/SW Co-design Workflow Summary

1. **HW Design**
   - Simulink Model

2. **IP Core Generation**
   - AXI Lite Accessible registers
   - Algorithm from MATLAB and Simulink

3. **Generate SW Interface Model**
   - SW Interface Model
   - Processor
   - AXI-Lite Bus

4. **SW Build**
   - FPGA Bitstream

5. **FPGA IP Core**
   - Algorithm from MATLAB and Simulink
   - External Ports

6. **SW I/O Driver Blocks**
   - SW Interface Model

7. **Embedded System Project**
   - Embedded System Integration

The workflow summary illustrates the process of developing a Zynq HW/SW co-design, starting with HW design, followed by IP core generation, generating SW interface models, and finally building SW and FPGA bitstream for the embedded system project.
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- Next Steps, Q&A
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