From High-Level Algorithms to ASML Automated Digital Design Flows

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May 21st, 2019 - Eindhoven
Key Takeaways

1. ASML business drivers: Quality and Time-to-Market, require an efficient workflow for getting smart algorithms into high speed digital hardware (FPGAs)

2. Adoption of Model-Based Design into the ASML Digital Design Flow achieves this with automatic generation of HDL source code and test bench code

3. Model-Based Design reduces the gap between system architect and design engineer
Chips are everywhere!
In 2015, 230 billion ICs were made, 30 for every man, woman and child on the planet.

IC units, in billions

Semiconductor Revenue Milestones

- $50B 1989
- $100B 1994
- $200B 2000
- $300B 2010
- $400B 2017
- $500B 2019

Data: WSTS
We develop and build lithography systems for manufacturing those IC’s

150 tons of precision equipment

works with single nano-meter precision:

Grass grows at a speed of 33 nano-meter per second
Moore’s Law means doing “More with Less”

Cray Super Computer 1976
30M$, 8 Mb, 5500 kg, 150 kW

2018
1000 $, 512 MB + GB flash, 200 g, <1W
The industry is driven by Moore’s law, which continues, through ideas and value creation.

Log Scale System Performance/Watt

- 2008
- 2018
- 2028

>2X /2.4 years

2X /2.4 years

Relative cost per function

This is what we’re doing it for!

¹Lisa Su, AMD, “Immersive era in consumer computing”, IEDM, dec 2017
²Gordon Moore, “Progress in digital integrated Electronics” International; Electronic Device Meeting,, IEEE, 1975, p p 11-13

ASML Market Research
Our systems enable the faster, better, cheaper chips of tomorrow.

- **PAS 2500/10**
  - Resolution: 900nm, 150mm 66wph

- **PAS 5500/60**
  - Resolution: 450nm, 200mm 48wph

- **XT:1400**
  - Resolution: 65nm, 300mm 145wph

- **NXT:1950i**
  - Resolution: 38nm, 300mm 190wph

- **AT:850**
  - Resolution: 110nm, 300mm 102wph

- **NXE:3400B**
  - Resolution: 13nm, 300mm 125wph

- **High NA EUV**
  - Resolution: <8nm, 300mm 185wph

Source: ASML Product specs, Market Research
ASML makes the machines for making IC’s
Electronic Development within D&E ASML

- EDEV Wilton USA
- EDEV San Diego USA
- EDEV Veldhoven The Netherland
- Embedded Logic Firmware
Goals and Challenges
Challenges

- Algorithms in Software
- Performance need
- Algorithm complexity

Trend

- Algorithms in Embedded Hardware (FPGA)
- Implementation complexity
- Increased performance

**Need:**
High level design and implementation workflow for FPGAs
Goals

1. One ASML common method of developing algorithms in FPGAs

2. Make modeling, simulation and code generation accessible for ELF engineer

3. Reduce the gap between system architect and ELF engineer
How we do it
ASML ELF Way-of-Working (WoW)

3rd party IP  HDL  Integration
Simulink HDL  GDB

Integration Verification

Minimal impact on existing WoW

GDB = Generic Design Block, HDL = Hardware Description Language
ASML ELF Way-of-Working, elaborated

1. Simulink Simulation Model
2. Generate RTL Code
3. Generate Verification Items
4. Generate Block Level TB
5. Block Level Simulation
ASML workflow to create algorithm subsystem, an example
Automated Build and Test

1. Buildfiles are used to automate the various tasks involved in the FPGA design flow

2. The “Build process” makes extensive use of (GNU) Make
Achievements and Outlook
Using HDL Coder in ELF projects

- **Established workflow within the entire ASML organization.**
  - IT team (IT4E) maintains development software and Linux servers for any ELF project
  - Standard use of HDL Code Generation in ELF Design Flow (DDM2/Bulidfiles)
  - Integrated with workflow for communication protocols (GDB), integration tool (QSYS/Platform designer/Vivado Block design), hardware interfaces (VHDL)

- **Improved development of Digital Signal Processing (DSP) functions (vs. handwritten RTL and/or Testbench)**
  - Easier to make changes in a late stage of the project without compromising quality
  - Especially suited for complex DSP functions

- **Future work: automatic FPGA-In-the-Loop (FIL)**
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