What's new in MATLAB and Simulink for Model-Based Design

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What’s New?

Simulink Release Notes

- **R2016a**
  - New Features, Bug Fixes, Compatibility Considerations

  - Simulation Analysis and Performance
    - Automatic Solver Option: Set up and simulate your model more quickly with automatically selected solver settings
    - One-Click Display: Click a signal line to display its summary or waveform
    - Simulation Metadata Diagnostics: Unde
    - Multi-Input Root-Import Mapping: Conn
    - Simulation for Mixed Targets: Simulate
    - Time Out feature for Performance Adv
    - Solver Profiler: Speed up simulation
    - Diagnostic Viewer performance improvement

  - Component-Based Modeling
    - Variant Source and Sink Blocks with Conditions
    - Scoping Simulink Functions: Call Simulink Functions
    - Simulink Units: Specify, visualize, and mask masking of units
    - Mask Dialog: Create masks with flexible mask images
    - Mask Images: Quickly add images to masks
    - Tracing Simulink Functions: Display co

Stateflow Release Notes

- **R2016a**
  - New Features, Bug Fixes, Compatibility Considerations

  - Smart Editing Guesses: Accelerate common editing tasks with just-in-time contextual prompts
  - Intelligent Chart Completion: Build charts faster with automatic addition of default transitions and creation of complementary state names
  - Simulink Units: Specify, visualize, and check consistency of units on chart interfaces
  - Output Logging: Log output signals for charts
  - JIT for Messages: Reduce model update time for messages with JIT compilation technology
  - API changes for commented objects
  - Stateflow model templates for common design patterns
  - UserData parameter available for storing values

- **R2015a SP1**
  - Bug Fixes

- **R2015b**
  - Bug Fixes
Model-Based Design Workflow

- Research
- Requirements
- Design
  - Modeling
    - Scheduling
    - Event modeling
    - Performance
- Implementation
  - C, C++
  - VHDL, Verilog
  - Structured Text
  - MCU
  - DSP
  - FPGA
  - ASIC
  - PLC
- Integration
- Test and Verification
- Management and Reporting
Model-Based Design Workflow

RESEARCH

REQUIREMENTS

DESIGN

MODELING

SCHEDULING

EVENT MODELING

PERFORMANCE

IMPLEMENTATION

C, C++

VHDL, Verilog

STRUCTURED TEXT

MCU DSP FPGA ASIC PLC

TEST AND VERIFICATION

MANAGEMENT AND REPORTING

INTEGRATION
Model-Based Design Workflow
Messages, Functions and Scheduling
New SimEvents
Discrete-event simulation engine for multidomain system models
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Discrete-event simulation engine for multidomain system models

How does communication delays effect your system performance?
CAN simulation with Simulink and SimEvents

Effects of Communication Delays on an ABS Control System

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CAN simulation with Simulink and SimEvents
CAN simulation with Simulink and SimEvents
CAN simulation with Simulink and SimEvents
CAN simulation with Simulink and SimEvents
CAN simulation with Simulink and SimEvents

Without background noise

Vehicle stops after 14.2 seconds
CAN simulation with Simulink and SimEvents

Without background noise
Vehicle stops after 14.2 seconds

With background noise
Vehicle stops after 15 seconds
Scheduler Example
Scheduler Example
Scheduler Example
Scheduler Example

Architectural Components

Functional Components

![Figure 1: Task Timing](image-url)
Model-Based Design Workflow
Fast Restart

Run consecutive simulations more quickly
Fast Restart

Run consecutive simulations more quickly
Fast Restart

Run consecutive simulations more quickly
Simulink - Faster consecutive simulations

Fast Restart
Automatic Solver Selection
Understanding the selected solver
Understanding the selected solver
Understanding the selected solver - Solver Profiler

Solver profiler detected dense groups of zero crossings in these regions:

1. Identify states that contributed to the majority of zero crossings in these regions.
2. Highlight each block in the model. Explore the zero crossing setting for the block.
3. Examine upstream blocks to identify potential modeling improvements.

During simulation, the solver used the maximum step size 99.37% of total simulation time. You can improve the simulation speed by increasing the maximum step size in the Solver pane of model configuration parameters.
Model-Based Design Workflow

- Research
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- Design
  - Modeling
    - Scheduling
    - Event modeling
  - Performance
- Implementation
  - C, C++
  - VHDL, Verilog
  - Structured Text
    - MCU
    - DSP
    - FPGA
    - ASIC
    - PLC
- Test and Verification
- Management and Reporting
Three-Way Model Merge
Report Generation

Chapter 2. Root System

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Description

The cruise controller was designed with Stateflow. To test the controller, we use a harness set of test vectors imported from Excel, and the outputs compared to expected results.
Chapter 2. Root System

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Description

PDF Performance: 15b Versus 16a

Report Time (hours)

Report Size (pages)
Model-Based Design Workflow

RESEARCH

REQUIREMENTS

DESIGN

Modeling

Scheduling
Event modeling

Performance

IMPLEMENTATION

C, C++

VHDL, Verilog

Structured
Text

MCU

DSP

FPGA

ASIC

PLC

TEST AND VERIFICATION

MANAGEMENT AND REPORTING

INTEGRATION
New Product! Simulink Test

Develop, Manage, and execute simulation-based tests

Test Case Templates

- **Simulation Test**
  - Input
  - Output
  - Assessment Criteria

- **Baseline Test**
  - Input
  - File
  - Expected Outputs
  - Assessment Criteria

- **Equivalence Test**
  - Input
  - Output
  - Assessment Criteria
New Product! Simulink Test

- Automatically generate Test Harness
New Product! Simulink Test

- Automatically generate Test Harness

- Test Sequence block
New Product! Simulink Test

- Automatically generate Test Harness
- Create Test Sequences
- Manage and Reporting
New Product! Simulink Test

- Automatically generate Test Harness
- Create Test Sequences
- Manage and Reporting
Real-Time testing with Simulink Real-Time
Real-Time testing with Simulink Real-Time
Model-Based Design Workflow
Questions!
Thanks!