Model-Based Design for Safety-Critical and Mission-Critical Applications

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Technical Marketing
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Safety-Critical Model-Based Design Workflow

- **Validate**
  - **Requirements**
  - **Simulink® & Stateflow®**
    - Trace: RMI
  - **Model**
    - Trace: Model/Code Trace Report
    - Real-Time Workshop® Embedded Coder™
    - Conformance: Model Advisor
  - **Source Code**
    - Embedded IDE Link XXX
  - **Object Code**
  - Conformance: PolySpace™ Products
  - Verify: SystemTest™

- **Verify**
  - SystemTest™
  - SLDV Property Proving Model Coverage
  - SLDV Test Generation Embedded IDE Link XXX

- **Adopting Model-Based Design**
  - within Aerospace and Defense
Requirements Process for Model-Based Design

- Functional, operational, and safety requirements
  - Exist one level above the model
  - Models trace to requirements
- Requirements validation - complete and correct
  - Simulation is a validation technique
  - Traceability can identify incomplete requirements
  - Model coverage can identify incomplete requirements
- Requirements based test cases
  - Test cases trace to requirements
Requirements trace example – view from DOORS® to Simulink

2.4 Integral Control and Limit
The integral control shall generate a surface command based on the attitude rate error computed by the rate control, integral error gain and the autopilot engage state. The total integral command shall be limited to not exceed the integral command limit. When the autopilot is not engaged, the integral command and internal state shall be held at zero.
Requirements trace example – view from Simulink to DOORS

Chapter 2. System - attitude_controller

Table 2.1. Block Requirements Table

<table>
<thead>
<tr>
<th>Name</th>
<th>Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cmd Limit</td>
<td>2.1.2 Parameters 00000022 #28</td>
</tr>
<tr>
<td></td>
<td>2.5 Surface Command and Limit 00000022 #21</td>
</tr>
<tr>
<td>Disp Gain</td>
<td>2.1.2 Parameters 00000022 #23</td>
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<tr>
<td></td>
<td>2.2 Attitude Control and Limit 00000022 #18</td>
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<td>Disp Limit</td>
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<td>2.2 Attitude Control and Limit 00000022 #18</td>
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<td>Disp_Cmd</td>
<td>2.1.1 Inputs 00000022 #22</td>
</tr>
</tbody>
</table>
Requirements based test trace example – view from Simulink Signal Builder block to DOORS
### Model coverage report example

#### Discrete integrator block "Integrator"

**Parent:** /attitude_controller

<table>
<thead>
<tr>
<th>Metric</th>
<th>Coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cyclomatic Complexity</td>
<td>3</td>
</tr>
<tr>
<td>Decision (D1)</td>
<td>100% (8/8) decision outcomes</td>
</tr>
</tbody>
</table>

**Decisions analyzed:**

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<tbody>
<tr>
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<tbody>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Condition</th>
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<th>0/401</th>
<th>0/401</th>
</tr>
</thead>
<tbody>
<tr>
<td>integration result &gt;= upper limit</td>
<td>50%</td>
<td>50%</td>
<td>50%</td>
<td>50%</td>
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<td>0/401</td>
<td>0/401</td>
<td>0/401</td>
</tr>
</tbody>
</table>

#### Logic block "Not engaged"

**Parent:** /attitude_controller

<table>
<thead>
<tr>
<th>Metric</th>
<th>Coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cyclomatic Complexity</td>
<td>0</td>
</tr>
<tr>
<td>Condition (C1)</td>
<td>100% (2/2) condition outcomes</td>
</tr>
</tbody>
</table>

---

The MathWorks Symposium adopting Model-Based Design within Aerospace and Defense
Requirements Process take-aways

- Early requirements validation
  - Eliminates rework typically seen at integration on projects with poor requirements

- Early test case development
  - Validated requirements are complete and verifiable which results in well defined test cases

- Requirements management and traceability
  - Requirements management interfaces provide traceability for design and test cases
Design Process for Model-Based Design

- Model-Based Design
  - Create the design - Simulink and Stateflow®
  - Modular design for teams - Model Reference
  - Model architecture/regression analysis - Model Dependency Viewer
  - Documented design - Simulink Report Generator
  - Requirements traceability using Simulink Verification and Validation™
  - Design conforms to standards using Model Advisor
Example detailed design including model reference and subsystems
Model dependency viewer

Dependency view: do178b_dhc2
02-May-2007 10:26:59
Example Model Advisor report

Model Advisor Report for 'attitude_controller'

Model version: 1.21
Generated on: 03-May-2007 10:35:27

42 of 45 Passed

- Check model, local libraries, and referenced models for known upgrade issues
  Passed
- Identify unconnected lines, input ports, and output ports
  Passed
- Check root model Import block specifications
  Passed
- Check solver for code generation
  Sample times for this model is unconstrained. If the model does not specify any sample times, consider setting its Periodic sample time constraint parameter to ensure sample time independent. Otherwise, set the parameter to Specified if the model will not be referenced.
- Identify questionable blocks within the specified system
  Check for blocks not supported by Real-Time Workshop.
  Done
Design Verification for Model-Based Design

- Requirements based test cases
  - Automated testing using SystemTest™ and Simulink Verification and Validation
  - Traceability using Simulink Verification and Validation
- Robustness testing and analysis
  - Built in Simulink run-time diagnostics
  - Formal proofs using Simulink Design Verifier™
- Coverage Analysis
  - Verify structural coverage of model
  - Verify data coverage of model
SystemTest for requirements based testing
SystemTest – example report

Data Plotting and expected results comparisons

Summary of results

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start Time</td>
<td>19-Apr-2007 05:40:38</td>
</tr>
<tr>
<td>Stop Time</td>
<td>19-Apr-2007 05:41:13</td>
</tr>
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<td>Iterations Completed</td>
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<tr>
<td>Iterations Passed</td>
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<tr>
<td>Iterations Failed</td>
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<tr>
<td>Final Status</td>
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Signal Builder and Assertion Blocks
Model coverage report example – signal ranges

<table>
<thead>
<tr>
<th>Hierarchy</th>
<th>Test 1</th>
<th>Test 2</th>
<th>Test 3</th>
<th>Test 4</th>
<th>Test 5</th>
<th>Test 6</th>
<th>Test 7</th>
<th>Test 8</th>
<th>Test 9</th>
<th>Test 10</th>
<th>Overall</th>
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<tr>
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<td>Min</td>
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<td>Min</td>
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<tr>
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</tbody>
</table>
Simulink Design Verifier – Coverage Test

Model

Test Report

Generated Test Cases
Simulink Design Verifier – Objective Test

Model with Constraints and Objectives

Test Report

Chapter 3. Test Cases / Counterexamples

Test Case 1

Summary
Length: 0.13 Seconds (4 sample periods)
Objective Count: 2

Objectives Reached At:

<table>
<thead>
<tr>
<th>Step</th>
<th>Time (s)</th>
<th>Objective 1</th>
<th>Objective 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
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</table>

Generated Input Data:

<table>
<thead>
<tr>
<th>Step</th>
<th>Time</th>
<th>Objective 1</th>
<th>Objective 2</th>
</tr>
</thead>
<tbody>
<tr>
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<td>0</td>
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<td>0.07</td>
<td>2</td>
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</tbody>
</table>

Done
Simulink Design Verifier – Property Proving

Model with Assumption and Objective

Property to be proven

Report

Chapter 2. Test/Proof Objectives

Table of Contents

Status

Verify True Output

Status

Table 2.1. Objectives having No Counterexamples of 20 or Fewer Steps

<table>
<thead>
<tr>
<th>#</th>
<th>Type</th>
<th>Model Item</th>
<th>Description</th>
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<tbody>
<tr>
<td>1</td>
<td>Assert</td>
<td>Assertion</td>
<td>Assertion &quot;Assertion&quot; assert</td>
</tr>
</tbody>
</table>

With the following active constraints:

Name | Constraint
---|------------
Assumption | (0 | 1)

Verify True Output

Objectives of: Assertion

<table>
<thead>
<tr>
<th>#</th>
<th>Status</th>
<th>Test Cases</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Undecidable</td>
<td>info</td>
<td>assert</td>
</tr>
</tbody>
</table>
Design Process take-aways

- Modular reusable implementations
  - Platform independent design
  - Scalable to large teams
- Consistent and compliant implementations
  - Common design language
  - Automated verification of standards compliance
- Efficient verification process
  - Develop verification procedures in parallel with design
  - Coverage analysis early in the process
  - Automated testing and analysis
Coding Process for Model-Based Design

- Automatic code generation
  - Real-Time Workshop Embedded Coder
- Traceability
  - HTML Code Traceability Report
- Source code verification
  - Complies with standards using PolySpace MISRA-C® checker
  - Accurate, consistent and robust using PolySpace™ verifier
Incrementally Generate Code

- Incremental code generation is supported via Model Reference
- When a model is changed, only models depending on it are subject to regeneration of their code

- Reduces application build times and ensure stability of a project’s code
- Degree of dependency checking is configurable
Add Links to Requirements

```c
/* DiscretePulseGenerator: '<Root>/clock'

* Requirements for '<Root>/clock':
  * 1. Clock period shall be consistent with chirp tolerance
*/
rtb_clock =
  (rtDWork.clockTickCounter < 1.0 &
   rtDWork.clockTickCounter >= 0) ?
  1.0 :
  0.0;
if (rtDWork.clockTickCounter >= 2.0-1) {
```

Requirements appear in the code
Code to Model Trace Report

Traceability Report for attitude_controller

Table of Contents
1. Eliminated / Virtual Blocks
2. Traceable Simulink Blocks / Stateflow Objects / Embedded MATLAB Scripts
   - attitude_controller
   - attitude_controller/private
   - attitude_controller_types.h

Eliminated / Virtual Blocks

<table>
<thead>
<tr>
<th>Block Name</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Root/Disp Gain</td>
<td>Import</td>
</tr>
<tr>
<td>Root/Rate FB</td>
<td>Import</td>
</tr>
<tr>
<td>Root/Active FB</td>
<td>Import</td>
</tr>
<tr>
<td>Root/Move Eng</td>
<td>Import</td>
</tr>
<tr>
<td>Root/Model Info</td>
<td>Masked SubSystem</td>
</tr>
<tr>
<td>Root/Surf Core</td>
<td>Output</td>
</tr>
<tr>
<td>C17/Empty SubSystem</td>
<td>Empty SubSystem</td>
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Traceable Simulink Blocks / Stateflow Objects / Embedded MATLAB Scripts

Root system: attitude_controller

<table>
<thead>
<tr>
<th>Object Name</th>
<th>Code Location</th>
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<tbody>
<tr>
<td>Root/Disp Limit</td>
<td>attitude_controller.c:129, 130</td>
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<tr>
<td>Root/Disp Gain</td>
<td>attitude_controller.c:81, 82</td>
</tr>
<tr>
<td>Root/Rate FB</td>
<td>attitude_controller.c:74, 75, 82, 83</td>
</tr>
<tr>
<td>Root/Move Eng</td>
<td>attitude_controller.c:138, 144</td>
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<tr>
<td>Root/Integrator</td>
<td>attitude_controller.c:13, 83, 84, 85</td>
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<tr>
<td></td>
<td>attitude_controller_private.h:46, 45</td>
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</tbody>
</table>
Simulink Integration with PolySpace Products

- **Input1**
  - Entries
  - Varying from -500 to 500

- **K1 and K2**
  - Constants
  - Can be tuned from -297 to 303

- **Math operations**
  - Divide, add, min/max, product, subtract, sum...

- **Lookup tables**
  - Maps, surfaces, algorithms, extrapolations
  - Adjusted, tuned

---

Overflow?

Division by Zero?
See results in the model

- Change the model
- Generate the production code
- Run PolySpace software

PolySpace detected an error here
(after having analyzed the generated code)
Coding Process takeaways

- Reusable and platform independent source code
- Traceability
- MISRA-C compliance
- Static verification and analysis
Integration Process for Model-Based Design

- Executable object code generation
  - ANSI® or ISO® C or C++ compatible compiler
  - Run-time libraries provided
- Executable object code verification
  - Test generation using Simulink Design Verifier
  - Capability to build interface for Processor-In-the-Loop (PIL) testing
  - Analyze code coverage during PIL
  - Analyze execution time during PIL
  - Analyze stack PIL

```
Requirements

Model

Source Code

Object Code

Embedded IDE
```

Verify: SystemTest
Embedded IDE Link XXX

Verify: SLDV Test Generation
Embedded IDE Link XXX

MathWorks Symposium
Adopting Model-Based Design within Aerospace and Defense
Processor-in-the-Loop (PIL) Verification
- Execute Generated Code on Target Hardware

Execution
- on host and target
- non-real-time

Communication via one of
- data link e.g. serial, CAN, TCP/IP
- debugger integration with MATLAB
Integration Process Takeaways

- Integration with multiple development environments
- Test cases and harnesses generated automatically
- Efficient processor in-the-loop test capability
Wrap-up

- Tools to support the entire safety critical development process
- Participation on SC-205/WG-71 committee for DO-178C
- Safety-Critical/DO-178B guideline document
  - Available to licensed customers with Real-Time Workshop Embedded Coder
  - Contact Bill Potter (bill.potter@mathworks.com) or Tom Erkkinen (tom.erkkinen@mathworks.com)