MATLAB EXPO 2017
KOREA
4월 27일, 서울
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Better than Hand – Generating Highly Optimized Code using Simulink and Embedded Coder

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Key Takeaways

1. Reduce costs by optimizing hardware resources
2. Create innovative products that maximize algorithm content
3. Expand benefits of code generation to more applications

“The advantages of Model-Based Design over hand-coding in C can’t be overestimated.” Kazuhiro Ichikawa, Ono Sokki

Ono Sokki Reduces Development Time for Precision Automotive Speed Measurement Device
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“Embedded Coder generates optimized code that is as good as we can write, and we’ve never had any problems with defects in the generated code.”
Dr. Robert Turner, ABB

ABB Accelerates the Delivery of Large-Scale, Grid-Connected Inverter Products with Model-Based Design
Challenges

- Difficult to embed sophisticated, state-of-the-art algorithms into low-cost production hardware
  - Limited ROM, RAM, stack, and clock speed
- Not always known a priori during design, what embedded device or resource is required
  - Need to experiment to find optimal implementation
- Hand coding is process bottleneck
  - Introduces bugs, adds delays, reduces design iterations
Solutions

Optimization Techniques:
1. Use optimal settings
2. Minimize data sizes
3. Target vector engines
4. Select best processor(s)
5. Reduce data copies
6. Reuse components
7. Thrift logic
1. Use Optimal Settings

Features: Embedded Coder Quick Start
2. Optimize Data Types

Features: Single Precision Converter
3. Target vector engines

Features: Code Replacements

/* DiscreteFir: '<S1>/Discrete_FIR Filter' */
ne10_fir_float_neon(&ex_fir_ne10_tut_DW.S, &rt produced, &output, in[76])
PIL Benchmark Results for ARM Cortex-A

Execution Time (μsecs)

- **ANSI, No Opt**: 410.7 μsecs
- **ANSI, Opt**: 185.5 μsecs
- **NE10, No Opt**: 16.8 μsecs
- **NE10, Opt**: 14.1 μsecs

Example: FIR Filter

Run Format: [ANSI or Ne10], [gcc no opt or gcc -02], ARM 1Ghz Cortex A8
4. Select best processor(s) for your application

- Portable code: any device for **algorithm code generation**

- Support packages for **target-specific** system executable generation
  - ARM … Zynq

- Hardware vendors offer their **own target packages**
  - ADI, Infineon, Microchip, NXP, Renesas, STMicro, TI, ...
Results for PMSM Motor Control for ARM cores
- Average and Max Execution Time
5. Reuse data

```c
void Subsystem(void)
{
    ... 
    for (i = 0; i < 100; i++) {
        Reuse[i] = 2.0F * Reuse[i] * 20.0F;
    }
    fcn3(&Reuse[0]);
}
```

Features: Reusable Storage Classes
6. Reuse components

Features: Subsystem Reuse and Simulink Functions
7. Thrift Logic (Clone)

Features: Simulink Clone Detection
7. Thrift Logic (Prove)

Features: Polyspace Code Prover
Solution Summary

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Simulink and Embedded Coder new features let you:

1. Reduce costs by optimizing hardware resources
2. Create innovative products that maximize algorithm content
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“When we generated code from our Simulink models with Embedded Coder, the team we handed it off to knew it was gold”
Maria Radecki, BAE Systems

BAE Systems Delivers DO-178B Level A Flight Software on Schedule with Model-Based Design
Additional Customer References and Applications

- Honeywell Aerospace, USA
  Certified Flight Control Processor

- FLIR Systems, USA and Sweden
  Thermal Imaging FPGA

- Festo AG, Germany
  Robotic PLC

- GM, USA
  Powertrain ECU

- Alstom Grid, UK
  HDVC Power DSP

- Baker Hughes, Germany
  Oil and Gas Drill Processor

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