Modeling and Implementing Software-Defined Radio Communication Systems on FPGAs

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Agenda

• Integrated Model-Based Design to Implement SDR on FPGA’s, highlighting:

  – Rapidly develop and verify a baseline transmitter and receiver using library blocks
  – Automatically generate HDL code and integrate the code with target hardware
  – Verify the design using HDL cosimulation and FPGA-in-the-loop on an FPGA Evaluation Kit

• Q&A
Software Defined Radio - Demo
Beacon Frame Receiver – SDR Demo
Software Defined Radio

Software Implementation

Data Source → Data Compression → Error Correction Encoding → Digital Modulation → Digital to Analog Converter → RF Frontend

Data Sink → Data Expansion → Error Correction Decoding → Digital Demodulation → Equalization, Timing and Syncronization → Analog to Digital Converter → RF Frontend

Hardware Implementation
Software Defined Radio

Data Source → Data Compression → Error Correction Encoding → Digital Modulation

Data Sink → Data Expansion → Error Correction Decoding → Digital Demodulation → Equalization, Timing and Synchronization → Analog to Digital Converter → RF Frontend

Digital to Analog Converter → RF Frontend

Air Channel

Hardware Implementation

Software Implementation
Some SDR systems (various vendors)

<table>
<thead>
<tr>
<th></th>
<th>USRP</th>
<th>USRP2</th>
<th>BEE2</th>
<th>KUAR</th>
<th>LYGTECH</th>
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<tbody>
<tr>
<td>RF bandwidth (MHz)</td>
<td>16</td>
<td>50</td>
<td>25</td>
<td>30</td>
<td>5, 7, 20 or 22</td>
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<tr>
<td>Processing partition</td>
<td>Off-board</td>
<td>Mixed</td>
<td>On-board</td>
<td>On-board</td>
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<td>Processing architecture</td>
<td>GPP</td>
<td>GPP FPGA</td>
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<tr>
<td>Connectivity</td>
<td>USB2</td>
<td>GigEthernet</td>
<td>USB Ethernet</td>
<td>USB Ethernet</td>
<td>Ethernet</td>
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<tr>
<td>No. of antennas or RF paths</td>
<td>4</td>
<td>2</td>
<td>16</td>
<td>2</td>
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<tr>
<td>Cost</td>
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<td>Strengths</td>
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<tr>
<td>Weaknesses</td>
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Implementing a Wireless Receiver on an FPGA

Build a Baseline QPSK Model
- Create Simulink executable model to explore design choices and determine baseline performance
- Use model to generate wireless test signal

Elaborate and Prototype the Design
- Designing the carrier and timing recovery loops for a QPSK receiver
- Verify the design with the wireless test signal

Implement on Target Hardware
- Convert the QPSK design to an implementation level model
- Generate HDL code and integrate with target hardware
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Build a Baseline QPSK Model

Steps to follow

1. Get the Design Specification
2. Build the Executable Testbench
3. Verify the Model
Design Specifications

Modulation: QPSK
Symbol Rate: 195 kilo-sym/sec
RRCOS Filter
  - Stopband Attenuation: 30 dB
  - Rolloff: 0.25;
  - Interp/Decim Factor: 8
Carrier Frequency: 432 MHz
Communications System Toolbox

The Communications System Toolbox extends Simulink to design and simulate the physical layer of communication systems and components.

- **Modulation**
  - AM, PM, FM, CPM, TCM
    - Hard Decision, Log Likelihood
- **Forward Error Correction**
  - Reed Solomon, Convolutional
- **RF Impairments**
- **Synchronization, Equalization**
Build the Executable Test Bench

Simulink Executable Model

Simulink Library Browser

Visualization
Verify the Model with AWGN Channel and BER Analysis

Establish Baseline

Simulated Results vs Theory

BERTool
Verify the Model
Generate Wireless Test Signal using MATLAB/Simulink SDR Interface

Communications Model

Gigabit Ethernet

MAT file

Spectrum Analyzer

E100

USRP2

N210
Implementing a Wireless Receiver on an FPGA

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Implement on Target Hardware
- Convert the QPSK design to an implementation level model
- Generate HDL code and integrate with target hardware
Elaborate and Prototype the Design

Steps to follow

1. Add more realistic impairments to the Basic QPSK Model
2. Design mitigation algorithms
3. Test design with real captured data
Wireless Channel Impairments

- Additive thermal noise
- Multipath fading
  - Not a concern here due to close-range line-of-sight communication
- Synchronization
  - Carrier phase/frequency offset
  - Symbol timing offset
  - Frame boundaries
Effect of Carrier Frequency Offset
Effect of Carrier Frequency Offset

Phase offset (deg): -20

Frequency offset (Hz): 0
Effect of Carrier Frequency Offset
Carrier Synchronization

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Implement on Target Hardware
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Algorithm Development Process

- Explore and discover
- Gain insight into problem
- Evaluate options, trade-offs

Requirements

Research & Design

- Design
- Test
- Elaborate

Test & Verification

Implementation

**Desktop**
- .dll
- .exe
- .c, .cpp

**Embedded**
- C
- VHDL / Verilog
- Structured Text
Solution: C and HDL Code Generation

- Design, execute, and verify algorithms in MATLAB
- Automatically generate C or HDL code
- Deploy generated code on hardware
Targeting HDL with an SDR Platform – Workflow Demo
Model-Based Design flow using Simulink

from Algorithm to FPGA Implementation
Thank You!