Simulation of sigma delta converter using MATLAB Simulink

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LEOS/ISAC/ISRO
Successive approximation, subranging, and flash converters are called nyquist-rate converters.

Sigma-delta A/D converters attain the highest resolution for relatively low signal bandwidths.
DIFFERENT TYPES OF SDM IMPLEMENTATION

- Single loop sigma delta modulators

- Multi stage noise shaping (MASH) sigma delta modulators
Effect of the digital filter on the noise bandwidth.

**OVER SAMPLING**

**Oversampling by K Times**

- Power

Average noise floor

\[ k \frac{F_s}{2} \quad k F_s \]

**The Digital Filter**

- Power

Digital filter response

Oversampling by K times

\[ \frac{F_s}{2} \quad k \frac{F_s}{2} \quad k F_s \]

**FFT diagram of a multi-bit ADC with a sampling frequency kFS.**
Block diagram of 1st order SDM

First order sigma-delta ADC block diagram
Digital and Decimation Filter

Diagram showing the process:
- Analog Input
  - Delta Sigma Modulator
  - 1-bit Data Stream
  - Digital Low-Pass Filter
  - Multi-bit Data
  - Decimation Filter
  - Output Data

Graphs:
- INPUT SIGNAL $x(n)$
- DECIMATION RATE $r(n)$
- OUTPUT SIGNAL $(x(n)r(n))$
Single loop 3\textsuperscript{rd} order sigma delta Matlab simulink model
2\textsuperscript{nd} order sigma delta
Mash 1-1 SDM

Periodogram Power Spectral Density Estimate

Frequency (Hz)

Power/frequency (dB/Hz)

X: 10
Y: 111.8

X: 20.03
Y: -7.149
Single loop 3rd order sigma delta
Mash 1-1-1 SDM

Periodogram Power Spectral Density Estimate

Power/frequency (dB/Hz)

Frequency (Hz)

X: 10
Y: 121.4

X: 19.98
Y: -8.408
4th order single loop sigma delta
MASH 2-2 SDM

Periodogram Power Spectral Density Estimate

Power/frequency (dB/Hz) vs. Frequency (Hz)

X: 9.999
Y: 151.1

X: 20.04
Y: 30.22
TWO STAGES OF FIR FILTERING

Fig. Frequency response of filter FIR1
SOFTWARE REFERENCE MODELING OF DECIMATION FILTER:

CASCADED INTEGRATED COMB (CIC) FILTER:

Fig. Frequency response of CIC filter
## Comparison with MASH & single loop SIGMA DELTA

### Table-I

<table>
<thead>
<tr>
<th>Order of SDM</th>
<th>Decimation Factor</th>
<th>SNR(dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1(^{st}) order</td>
<td>1024</td>
<td>88</td>
</tr>
<tr>
<td>2(^{nd}) order</td>
<td>512</td>
<td>104</td>
</tr>
<tr>
<td>3(^{rd}) order</td>
<td>256</td>
<td>120</td>
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<tr>
<td>4(^{th}) order</td>
<td>128</td>
<td>121</td>
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</table>

### Table-II

<table>
<thead>
<tr>
<th>Order of Mash SDM</th>
<th>Decimation Factor</th>
<th>SNR(dB)</th>
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</thead>
<tbody>
<tr>
<td>Mash 1-1</td>
<td>256</td>
<td>118</td>
</tr>
<tr>
<td>Mash 1-1-1</td>
<td>128</td>
<td>129</td>
</tr>
<tr>
<td>Mash 2-2</td>
<td>64</td>
<td>120</td>
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</table>
Conclusion & Future work

- Single loop SDM comparator overloading and stability of the system limit the overall SNR.
- Here feed forward architecture used because of better linearity.
- MASH SDM overall performance is comparable with single loop SDM at lower OSR.
- LEOS has realized MASH1-1-1 structure using discrete rad-hard component.
- Overall MASH, and SDM model realized first using MATLAB SIMULINK and MATLAB FDA Tool.
REFERENCES


[3] Babita Roslind, *Design Techniques For Sigma-Delta Based Adc For Wireless Applications* Jose


[7] Yung-Fu Lin, *Design of Multi-Stage Noise Shaping Sigma-Delta Modulator*


[9] XIAOLONG YUAN, *Wideband Sigma-Delta Modulators*