New Techniques for Verification, Validation, and Test

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Verification, Validation and Test

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Simulink Design Verifier

Generating tests for model coverage or user defined objectives

Simulink and Stateflow models

Simulink Design Verifier

Test Generation

Test Harness with Signal Inputs
VV&T Process Formality

- Modeling & Simulation
- Testing Early & Often
- Driving Process with Requirements
- Safety Critical

Certified
“Formal”
“Informal” Requirements

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VV&T Products before 2006

- Modeling & Simulation
- Testing Early & Often
- Driving Process with Req’s
- Safety

Simulink Verification & Validation
- xPC Target
- Link for Code Composer Studio
- Link for ModelSim
New VV&T Products in the Last Year

Modeling & Simulation

- xPC Target
  - Link for Code Composer Studio
  - Link for ModelSim

Testing Early & Often

- Simulink Verification & Validation
- PolySpace
  - Link for TASKING
  - Link for Analog Devices VisualDSP++
  - Link for Cadence Incisive

Driving Process with Req’s

- Simulink Design Verifier
  - Modeling Standards Checker
    - (Simulink Verification & Validation)

Safety

Consulting
New VV&T Products in the Last Year

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- SystemTest
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- Simulink Design Verifier
- Consulting

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SystemTest 1.1

*Manage tests and analyze results for system verification and validation*

- Uses
  - Stress testing
  - Parameter sweeps
  - Monte Carlo simulation
  - Algorithm verification & validation

- Model verification & validation
  - Vary block parameters
  - Measure and report model coverage (with Simulink Verification & Validation)
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VV&T: More To Come in the Future

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