MODELLING NEAR FIELD COMMUNICATION SYSTEMS AND IMPLEMENTATION ON ASIC

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What Is Near Field Communication (NFC)?

Components of an NFC System

Developing an NFC System Using Mathematical Analysis and Modelling Software Tools

Moving from Model to RTL for FPGA and ASIC

Conclusion
WHAT IS NEAR FIELD COMMUNICATION (NFC)?
WHAT IS NFC?

- NFC is an ecosystem of tags and readers for travel, commerce, door entry, and many other applications.
- It’s a short-range, intuitive touch or swipe use model (within a few cm).
- Current interest is mainly in mobile applications using the handset as a platform.
WHAT IS NFC?

- A concept similar to RFID, but extended—an NFC Forum device is capable of operating in Peer-to-Peer mode or as a Reader/Writer, as well as emulating NFC Forum Tags or Contactless Cards (optional).

- NFC is overseen and specified by the NFC Forum, but its constituent standards come from individual groups, such as ISO. To quote the NFC Forum:
  - A standards-based connectivity technology, NFC harmonizes today’s diverse contactless technologies, enabling current and future solutions in areas such as:
    - Access control
    - Consumer electronics
    - Healthcare
    - Information collection and exchange
    - Loyalty and coupons
    - Payments
    - Transport

Source: NFC Forum (www.nfc-forum.org)
WHAT IS NFC?

- A simple and intuitive concept, but by no means a trivial system:
  - Three possible modes of operation: tag, reader, peer-to-peer
  - Multiple RF Standards (ISO 14443-2,3,4; ISO 18092; JIS X6319-4)
  - Several digital protocols and standards for data exchange (LLCP, NDEF)
  - Four different data rates
  - Four different tag types
  - Uses EMVCo* for payment applications

- The goal is to bring all this to your mobile phone and other devices:

* EMVCo is owned by American Express, JCB, MasterCard, and Visa.
COMPONENTS OF AN NFC SYSTEM
SIMPLIFIED NFC SYSTEM BLOCK DIAGRAM
SOME COMPONENTS OF AN NFC SYSTEM

- **Antenna, usually a coil, connected through a matching network**
  - Two coupled coils produce challenging resonance and distortion effects.

- **RF front end operating at 13.56 MHz**
  - **Tag Mode**: Possible to operate with a discharged battery using the Reader’s field power, so there is an optional power harvesting block.
  - **Reader/Writer Mode**: Antenna driver must be capable of delivering power as well as the modulated data to a tag.

- **Modulators**
  - **Tag Mode**: Uses load modulation in various formats, depending on the standard.
  - **Reader Mode**: Mostly uses ASK of various depths and in several formats.
SOME COMPONENTS OF AN NFC SYSTEM

- **Demodulators**
  - Complementary to the modulators, in a variety of formats.
  - Very large carrier to modulation ratio requires some innovative design.

- **Digital Controller and Host Interface**
  - Can include interfaces to secure elements and SIMs.

- **Mathematical analysis and modelling software tools are useful for designing many of these blocks, or subblocks within them.**
GENERALISED DESIGN FLOW

NFC Forum Standards

Algorithm Design → Time Domain Simulation → RTL Generation

Modelling Tools

RTL Generation → FPGA Emulation → ASIC

Mathematical analysis and modelling software

Modelling Tools

Bug Fixes → Modelling Tools
What the appropriate use of the right tools brings to the development process:

**Algorithm development — Mathematical Analysis**
- Provides a higher level or more abstract exploration of ideas (e.g., techniques to overcome channel impairments).
- Useful for getting specific algorithms right and to thoroughly understand the math (e.g., application of a certain transform to a data set).

**Algorithm development — Modelling Tools**
- Used for signal flows, loops, and moving algorithms from floating to fixed-point representation (e.g., control loops, fixed-point filter performance).
- Embedded Function Blocks are very helpful when it is more intuitive to write small chunks of code (e.g., encoders, decoders, and state machines).
- Libraries are helpful for reuse of blocks and collaborative working (e.g., I and Q channels are duplicates, so we want a change in one to be reflected in the other).
What the appropriate use of the right tools brings to the development process (Continued):

- **Toolboxes and Block Sets** (e.g., DSP System, SimPowerSystems)
- **System performance—Modelling Tools and Mathematical Analysis**
  - Simulate the complete design as a software model to gather performance data (e.g., error rate).
  - Dumping data for postprocessing and analysis can be faster but needs more memory.
MATLAB FUNCTION BLOCKS

- Ideal for small encoding tasks or state machines.
- If written appropriately, function blocks are compatible with HDL Coder tools.
LIBRARIES FOR BLOCK REUSE

- Changes to the library blocks are automatically reflected in the actual design—makes design consistency easier.
- A good repository for frequently used blocks—the multiple protocols and formats used by NFC have similar functions occurring several times.
- Library blocks can take parameters.
- Suppose several colleagues are evaluating the same block in different test benches.
- Using libraries (with additional version control, e.g., SVN, CVS) is an easy way to avoid manual merging of designs and to ensure that the latest changes are in place.
MODELLING ANALOGUE PARTS OF THE SYSTEM

- NFC works on the basis of inductive coupling.
- When acting as a Reader, maximum power must be transferred through the matching network into the antenna and on to the passive tag, but without disrupting the received modulation.
- Use the SimPowerSystems library to model this and evaluate it in a system context.
- SimPowerSystems also helps with the design of other digital blocks by enabling signals from the analogue domain to be appropriately simulated.
- Some of the benefits of cosimulation but in one tool.
MOVING FROM MODEL TO RTL FOR FPGA AND ASIC
Once a design (e.g., Reader Demodulator) is complete and running successfully in one or more test benches, RTL is required for the next stage of testing in FPGA.

Hand-coding bit- and cycle-exact Verilog or VHDL is tedious and prone to errors, but HDL Coder tools make things very quick and easy: just a few configurations and press the button.

Machine-generated code provides high confidence that the RTL and the design match very closely.

FPGA evaluation allows real-time live testing of the design in the context of the rest of the system—i.e., analogue front end, other hand-coded RTL, real tags.

Strange/unexpected/erroneous behavior can be investigated by capturing signals and feeding them back into the model.

Revised RTL from bug fixes or design modifications can be generated very quickly; take as many iterations at the FPGA stage as are necessary.
Data captured from the FPGA test platform (e.g., using a digital scope) can be used to stimulate the design.

Repeating Sequence Stair is a convenient block to use for data of a single dimension; there are also other ways.
CONCLUSION
Apart from the obvious features of data manipulation and plotting, the main benefits for the design and production of the NFC ASIC are:

- Fixed-point support in modelling software, coupled with HDL Coder tools, which make generation of bit- and cycle-exact RTL very quick and straightforward.
  - Debugging can be done using captured FPGA data.
- Aids to system design are available, such as DSP Systems (formerly Filter Design Toolbox).
- There’s a single tool to model and evaluate analog circuits as well as algorithmic blocks, using the SimPowerSystems block set.