FPGA-Based Rapid Control Prototyping of Permanent Magnet Synchronous Motor Servo Drives

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Key Takeaways
- Experimental results of multi-rate controller for a PMSM
- Outer loop: LQR position controller with disturbance observer
- Inner loop: field-oriented control of stator currents
- Real-time testing using multi-core CPUs and a Xilinx FPGA
- Automatic C and VHDL code generation from Simulink

Abstract
The position control problem in permanent magnet synchronous machine (PMSM) drives is a challenging problem which is subject to tight time constraints and unknown disturbances. This paper presents experimental validation of a cascade control structure for position control in PMSM drives. A PI-based control algorithm is used in the inner loop to control the stator currents in the rotor d-q reference frame. Then an optimal controller is synthesized in the error space of the outer loop to control the position and velocity of the PMSM. A disturbance observer is employed to estimate the load torque and parameter mismatch of the drive and a control algorithm is deployed on a real-time system with a field-programmable gate array (FPGA) board, thereby performing an experimental validation in real-time.

Introduction
The position control problem in PMSM drives is challenging due to tight time constraints and unknown disturbances. For best results, the control in PMSM drives is usually done through field-oriented control (FOC) [3] in the rotor d-q reference frame [4]. The basic idea of FOC is to control the torque and flux in a similar manner with the DC machine. It yields a cascade control solution with two inner loops for current control and outer velocity and position control loops [5].

Permanent Magnet Synchronous Machine
The PMSM mathematical model in the rotor d-q reference frame is given by the following equations [4]:

\[ v_d(t) = R_d i_d(t) + L_d \frac{di_d(t)}{dt} - \omega(t) L_q i_q(t) \]  \hspace{1cm} (1a)

\[ v_q(t) = R_q i_q(t) + L_q \frac{di_q(t)}{dt} + \omega(t) L_d i_d(t) \] \hspace{1cm} (1b)

\[ T_e(t) = \frac{3p}{2} \left( \lambda_m i_q(t) + (L_d - L_q)i_d i_q \right) \] \hspace{1cm} (1c)

\[ \frac{d\omega(t)}{dt} = \frac{T_e(t) - diti_d(t) - T_L(t)}{J_m} \] \hspace{1cm} (1d)

\[ \frac{d\theta(t)}{dt} = \omega(t) \] \hspace{1cm} (1e)

Challenge
For a PMSM-based servo system, synthesize a position and velocity control algorithm with the following properties: (1) fast convergence to the reference, (2) disturbance rejection and (3) low computational complexity that fits typical FPGA or microcontroller specifications.

Control Strategy
The multi-rate cascaded control structure is depicted in the figure below and it is composed of:
1) Current control inner-loop based on field-oriented control, and
2) Position control outer-loop using a linear quadratic regulator (LQR)

\[ u = Kx - x_{ref} + u_{ref} \]

with \( u_{ref} \) being related to the reference input feedforward, and \( x \) and \( x_{ref} \) being the measured and reference states of the equations of motion for the control outer-loop. The load torque is unknown but required for the input feedforward \( u_{ref} \). A disturbance observer is derived to solve the tracking control problem.

Real-Time Implementation
A multi-rate cascade control structure is used to control the PMSM rotor position. The motor currents are controlled through the inner control loop with a faster sample rate \( T_f \) while the position tracking is controlled via the outer control loop running with a slower sample rate \( T_s \). Furthermore, the PWM signal generation and incremental quadrature encoder measurements need to run at a very fast sample rate \( T_{FPGA} \).

Baseline real-time target machine

CPU (4 cores)
Artix-7 FPGA
Field- Oriented Control and Torque Observer
@ 80 µs execution

Figure – Cascade control structure

Figure – Diagram of PMSM control architecture

The load torque estimation and the inner closed-loop is implemented with a sample time of 80 µs. The actual rotor position is obtained from an incremental quadrature encoder fitted to the motor shaft. The controller provides a reference duty-cycle for the 3-phase PWM generator running in the FPGA.
Hardware Implementation

The cascade control structure is modeled in Simulink and deployed to a Speedgoat real-time system. The latter consists mainly of two components:

a) Baseline real-time target machine with a quad core CPU
b) IO397 Simulink-programmable FPGA I/O module with a Xilinx Artix®-7 FPGA connected to 8 analog inputs, 8 analog outputs and 14 digital I/O

Code is automatically generated from the Simulink models to the CPU or FPGA by using Simulink Real-Time” or HDL Coder™, respectively. The experimental setup is depicted on the right.

Experimental Results

The tracking performance of the position control is tested with a step change of 180 degrees. The position results are shown in the figures below. The LQR controller (green solid lines) can be optimized to obtain smooth and fast transient response. When a constant disturbance is applied after around 2.1 seconds, the LQR controller (green solid lines) has a better disturbance rejection than the PID controller (red dotted lines), both for transient and steady-state conditions.

Conclusion

This paper discusses a multi-rate controller architecture to control angular position of a PMSM. An LQR position controller with a disturbance observer is derived and modelled in Simulink. A PID controller is also modelled for comparison purposes. The Simulink model of the control architecture is deployed to a Speedgoat real-time target machine with a multi-core CPU and a Xilinx FPGA, that is in turn connected to a PMSM drive and motor. With the proposed rapid control prototyping setup, the Simulink-based model could be later deployed to a microcontroller or FPGA for final production. Experimental results demonstrate the improved disturbance rejection of the LQR controller.

References